VIA Eden V4 Micro Module

User's Manual

1st Ed – 23 August 2006

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THIS DEVICE COMPLIES WITH PART 15 FCC RULES. OPERATION IS SUBJECT TO THE FOLLOWING TWO CONDITIONS:

(1) THIS DEVICE MAY NOT CAUSE HARMFUL INTERFERENCE.

(2) THIS DEVICE MUST ACCEPT ANY INTERFERENCE RECEIVED INCLUDING INTERFERENCE THAT MAY CAUSE UNDESIRED OPERATION.

THIS EQUIPMENT HAS BEEN TESTED AND FOUND TO COMPLY WITH THE LIMITS FOR A CLASS "A" DIGITAL DEVICE, PURSUANT TO PART 15 OF THE FCC RULES.

THESE LIMITS ARE DESIGNED TO PROVIDE REASONABLE PROTECTION AGAINTST HARMFUL INTERFERENCE WHEN THE EQUIPMENT IS OPERATED IN A COMMERCIAL ENVIRONMENT. THIS EQUIPMENT GENERATES, USES, AND CAN RADIATE RADIO FREQUENCY ENERGY AND, IF NOT INSTATLLED AND USED IN ACCORDANCE WITH THE INSTRUCTION MANUAL, MAY CAUSE HARMFUL INTERFERENCE TO RADIO COMMUNICATIONS.

OPERATION OF THIS EQUIPMENT IN A RESIDENTIAL AREA IS LIKELY TO CAUSE HARMFUL INTERFERENCE IN WHICH CASE THE USER WILL BE REQUIRED TO CORRECT THE INTERFERENCE AT HIS OWN EXPENSE.

Notice

This guide is designed for experienced users to setup the system within the shortest time. For detailed information, please always refer to the electronic user's manual.

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- 4. Carefully pack the defective product, a complete Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
- 5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

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1. Getting Started

1.1 Safety Precautions

Warning!



Always completely disconnect the power cord from your chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.

Caution!



Always ground yourself to remove any static charge before touching the CPU card. Modern electronic devices are very sensitive to static electric charges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components in a static-dissipative surface or static-shielded bag when they are not in the chassis.

1.2 Packing List

Before you begin installing your single board, please make sure that the following materials have been shipped:

- 1 x ECM-3711 VIA Eden ESP10K micro module
- 1 x Quick Installation Guide for ECM-3711
- 1 x AUX-001 daughter board
- 1 x CD-ROM or DVD-ROM contains the followings:
 - User's Manual (this manual in PDF file)
 - Ethernet driver and utilities
 - VGA drivers and utilities
 - Audio drivers and utilities
- 1 x Cable set contains the followings:
 - 1 x IDE HDD cable (40-pin, pitch 2.54mm)
 - 1 x Serial port cable (9-pin Mini DIN-Dupont 10-pin/2.0mm)
 - 1 x Audio cable (10-pin, pitch 2.0mm)
 - 1 x USB cable (Dupont 10-pin/2.54mm-10pin/2.0mm)
 - 1 x PS/2 Keyboard & mouse Y cable (6-pin, Mini-DIN)
 - 2 x Serial ATA cable (7-pin, standard)



If any of the above items is damaged or missing, contact your retailer.

1.3 Document Amendment History

Revision	Date	Ву	Comment
1st	Aug. 2006	Jason Liu	Initial Release

1.4 Manual Objectives

This manual describes in detail the Evalue Technology ECM-3711 Single Board.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of this board.

We strongly recommend that you study this manual carefully before attempting to interface with ECM-3711 series or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

Please be aware that it is possible to create configurations within the CMOS RAM that make booting impossible. If this should happen, clear the CMOS settings, (see the description of the Jumper Settings for details).

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Customer Service department with the relevant details.

1.5 System Specifications

System 😌		
CPU	Onboard VIA Eden V4 1 GHz	
BIOS	Award 512 KB Flash BIOS	
System Chipset	VIA CN700/VT8251	
I/O Chip	VIA VT1211	
System Memory	One 200-pin SODIMM supports up to 1 GB DDR2 400/533 SDRAM	
SSD	One CompactFlash Type I/II socket	
Watchdog Timer	Reset: 1~255 min. and 1 sec./step	
H/W Status Monitor	Monitoring system temperature, voltage, and cooling fan status. Auto	
	throttling control when CPU overheats.	
Expansion	One Mini-PCI slot	
1∕0 ☉		
MIO	2 x EIDE (Ultra DMA 100), 2 x SATA, 1 x RS-232, 1 x RS232/422/485, 1 x	
	K/B & Mouse	
IrDA	115k bps, IrDA 1.0 compliant	
DIO	16-bit General Purpose I/O for DI and DO	
USB	4 x USB 2.0 ports	
Display 오		
Chipset	VIA ProSavage CN700 integrated 2D/3D gaphic engine	
Display Memory	64 MB frame buffer using system memory	
Resolution	CRT mode: 1600 x 1200 @ 24 bpp (60 Hz)	
	LCD/Simultaneous mode: 1600 x 1200 @ 24 bpp (60 Hz)	
LVDS	Dual-channel 18/24-bit LVDS	
Audio 오		
Chipset	VIA VT8251	
AC97 Codec	VIA VT1616 supports 5.1 CH Audio	
Audio Interface	Mic in, Line in, CD Audio in, Line out	
Ethernet 😌		
Chipset	Dual Realtek RTL8111B	
Ethernet Interface	1000Base-T Fast Ethernet compatible	

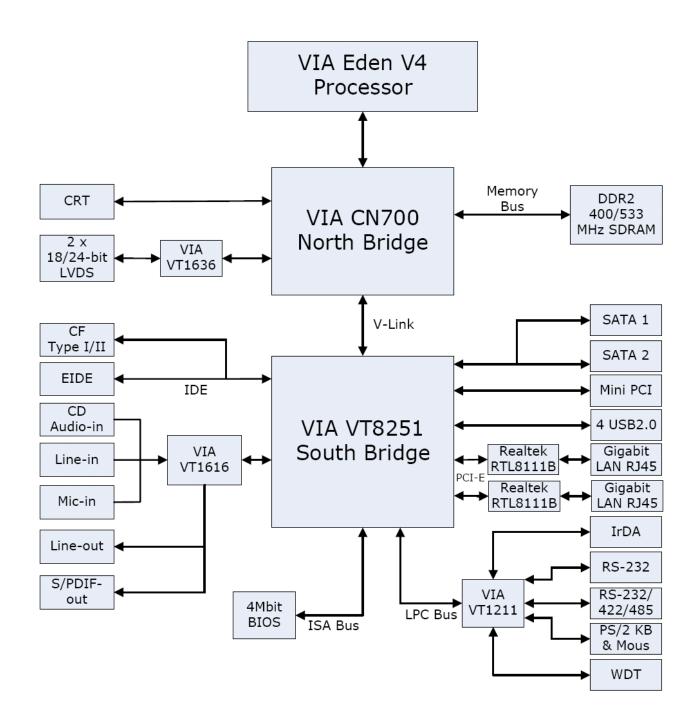
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Mechanical & Environmental	\odot
Bower Boguirement	+5 V @ 4.63 A, +12 V @ 0.53 A, 5 Vsb @ 0.32 A (with VIA Eden V4 1
Power Requirement	GHz & 1 GB DDR2 SDRAM)
Power Type	ATX
Operation Temperature	0~60°C (32~140°F)
Operating Humidity	0%~90% relative humidity, non-condensing
Size (L x W)	45.7" x 4" (146 mm x 101 mm)
Weight	0.51 lbs (0.23 kg)

1.6 Architecture Overview

1.6.1 Block Diagram

The following block diagram shows the architecture and main components of ECM-3721 Series.



The following sections provide detail information about the functions provided onboard.

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1.6.2 VIA CN700 & VT8251

The CN700 implements a deep In-Order Queue to improve system performance for multi-threaded software applications. DBI and V4 bus protocol are supported which effectively reduce overall system power consumption. The AGP controller is AGP v3.5 compliant with up to 2.1GB/second data transfer rate. It supports pseudo-synchronous AGP and CPU interface to maximize system performance. Deep read and write (256 bytes each) FIFO are integrated for optimal bus utilization and minimum data transfer latency. The CN700 supports 64-bit memory data bus access and the DDR DRAM interface allows zero wait-state data transfer bursting between the DRAM and memory controller's data buffers. The different banks of DRAM can be composed of an arbitrary mixture of 64 / 128 / 256 / 512 / 1024 Mb SDRAM in x 8 or x16 configurations. The DRAM controller can run either synchronous or pseudo-synchronous with the host CPU bus. The CN700 North Bridge interfaces to the South Bridge through a high speed (up to 533 MB/sec) 8x 66 MHz Data Transfer interconnect bus called V-Link interface. Deep pre-fetch and post-write buffers are included to allow for concurrent CPU and V-Link operation. System Power Management for sophisticated power management, the CN700 supports dynamic CKE control to minimize DDR SDRAM power consumption during normal system state (S0). A separate suspend power plane is implemented for the memory control logic for Suspend-to-DRAM state. The CN700 graphics controller implements dynamic clock gating for inactive functions to achieve maximum power saving. The system can be switched to standby or suspend states to further reduce power consumption when idle. VESA DPMS (Display Power Management Signaling) CRT power-down is supported. 3D Graphics Engine Featuring an integrated 128-bit 3D graphics engine, the CN700 North Bridge utilizes a single cycle architecture that provides high performance along with superior image quality. Several new features enhance the 3D architecture, including single-pass multitexturing, anisotropic filtering, and an 8-bit stencil buffer. The chip also offers the industry's only simultaneous usage of single-pass multitexturing and single-cycle trilinear filtering – enabling stunning image quality without performance loss. Image quality is further enhanced with true 32-bit color rendering throughout the 3D pipeline to produce more vivid and realistic images. The advanced triangle setup engine provides realistic user experiences in games and other interactive 3D applications. The 3D engine is optimized for AGP texturing from system memory.

• 2D Graphics Engine

The CN700 North Bridge's advanced 128-bit 2D graphics engine delivers high-speed 2D acceleration for productivity applications. The enhanced 2D architecture with direct access frame buffer capability optimizes UMA performance and provides acceleration of all color depths. MPEG Video Playback The CN700 North Bridge provides the ideal architecture for high quality MPEG-2 based video applications. For MPEG playback, the integrated video accelerator offloads the CPU by performing the motion compensation tasks, while its enhanced scaling algorithm delivers incredible full-screen video playback. The CN700 provides three "Digital Video Port" interfaces: FPDP, GDVP1, and DVP0. The Flat Panel Display Port (FPDP) implements a 24-bit / dual 12-bit interface which is designed to drive a Flat Panel Display via an external LVDS transmitter chip. The CN700 can be connected to the external LVDS transmitter chip in either 24-bit or dual-12-bit modes. A wide variety of LCD panels are supported including VGA, SVGA, XGA, SXGA+ and up to UXGA-resolution TFT color panels, in either SDR (1 pixel / clock) or DDR (2 pixels / clock) modes. Two 12-bit "Display Port" interfaces are provided (through multiplexing with AGP interface) plus a dedicated 12-bit display port interface. Multiplexing display functions with the AGP bus allows embedded systems to support an external AGP connector for future performance upgrade through the external graphics controller. It also allows add-in cards to be designed with an AGP-compatible connector for implementing the display interface logic to reduce cost in the base (CRT-only) configuration. In the value system configurations, the external AGP upgrade capability is not normally required by the system, allowing all the AGP pins to be used for implementing very flexible display functions.

Internally the CN700 North Bridge provides two separate display engines, so if two display devices are connected, each can display completely different information at different resolutions, pixel depths and refresh rates. If more than two display devices are connected, the additional displays must have the same resolution, pixel depth and refresh rate as one of the first two. The maximum display resolutions supported for one display device are listed in the table below. If more than one display is implemented (i.e., if both display engines are functioning at the same time), then available memory bandwidth may limit the display resolutions supported on one or both displays. This will be dependent on many factors including primarily clock rates and memory speeds (contact VIA for additional information).

The VT8251 interfaces to the companion North Bridge chip through the Ultra V-Link interface with up to 1 GB/sec data transferrate. Two 1-Lane PCI Express ports are provided for high-speed peripheral devices. The VT8251 allows combining the two 1-Lane PCI-E ports into a 2-Lane port for peripheral that requires extra bandwidth. For standard 33 MHz PCI devices, the VT8251 supports up to seven PCI master devices.

In addition, the VT251 integrates extensive peripheral controllers for modern, state-of-the-art PC systems:

• Four-port Serial ATA / RAID Controller

The Serial ATA / RAID controller supports RAID Level 0, RAID Level 1, RAID Level 0+1 and JBOD, and complies with Serial ATA Specification Revision 1.0, and Serial ATA II specification. The Serial ATA controller is configurable and can be configured to support either 4 Serial ATA II master ports or 2/2 Serial ATA I master/slave ports with 3.0 Gbits/sec and 1.5 Gbits/sec data transfer rates.

Dual-channel Enhanced IDE Controller

In addition to standard PIO and DMA mode operation, the VT8251 also supports the UltraDMA-133, 100, 66, and 33 standards, allows reliable data transfer rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

- IEEE 802.3 compliant 10 / 100 Mbps Ethernet MAC with MII interface to external PHYceiver
- Universal Serial Bus Controller with eight USB 2.0 ports

The VT8251 USB controller includes four USB 1.1 root hubs, a USB 2.0 root hub, and eight USB 2.0 ports with integrated physical layer transceivers. Hot plug and isochronous peripherals are supported. Support of legacy keyboard and mouse is implemented so that legacy software could run transparently.

Integrated AC97-link Controller

The AC-link controller can be used to attach an audio codec (AC), a modem codec (MC), an audio modem codec (AMC) or a combination of ACs and a single MC.

- Full System Management Bus (SMBus) interface
- Keyboard controller with PS/2 mouse support
- Real Time Clock with 256 bytes extended CMOS

In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field and other enhancements for compatibility with the ACPI standard.

 Notebook-class, sophisticated Power Management Unit compliant with ACPI and legacy APM requirements

Multiple sleep states (POS, STR and STD) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop, PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

• Plug and Play functions with steerable PCI interrupts

The PnP function allows complete steerability of PCI interrupts and integrated peripheral interrupts to system interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and re-configurability of on-board peripherals for Windows family compliance.

The VT8251 also enhances the functionality of standard integrated peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type-F DMA in addition to standard ISA DMA modes. Compliant with the PCI v2.3 specification, the VT8251 supports delayed transactions so that slower internal ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing deadlock in a PCI-to-PCI bridge environment.

1.6.3 VIA VT1616 AC'97 Codec

VIA Technologies' VT1616TM 18-bit audio codec conforms to the AC'97 2.2 and S/PDIF output specifications. The VT1616 integrates Sample Rate Converters on all channels and can be adjusted in 1Hz increments. There is a provision in hardware for down-mixing the 6 channels into stereo when only two end points are available. The analog mixer circuitry integrates a stereo enhancement to provide a pleasing 3D surround

sound effect for stereo media. This codec is designed with aggressive power management to achieve low power consumption. When used with a 3.3V analog supply, power consumption is further reduced. The primary applications for this part are desktop and portable personal computers multimedia subsystems. However, it is suitable for any system requiring 6-channel audio output for home theater systems at competitive prices.

- AC'97 2.2 S/PDIF extension compliant codec
- 18-bit, 6 channel DAC outputs
- 1Hz resolution VSR on all channels
- Integrated IEC958 line driver for S/PDIF
- S/PDIF compressed digital or LPCM audio out
- Hardware downmixoption to 2 channels
- 3D stereo expansion for simulated surround
- 18-bit independent rate stereo ADC
- 4 stereo, 2 mono analog line-level inputs
- Second line-level output with volume control
- External Audio Amplifier Control
- Low Power consumption mode
- Exceeds MicrosoftR WHQL logo requirements
- 3.3V digital, 3.3 or 5V analog power supply
- 48-pin LQFP small footprint package

1.6.4 VIA VT1636 LVDS Transmitter

- Support Single / Dual LVDS Transmitter Function
- Compatible with TIA/EIA-644 LVDS Standard
- Supports LVDS 18-bit and 24-bit Output
- Supports Dual Channel UXGA Panel Display
- Supports 2D Dither for 18-bit Panel
- Supports Option for 24-bit Color Mapping with Convertional (LSB) or Non-Conventional (MSB) Format Output
- Supports DVO Input Mode with 25 to 165 MHz Input Clock
- Programmable Input Clock and Strobe Select
- Narrow bus Reduces Cable Size and Cost
- PLL equires No External Components
- Two-Wire Serial Communication
- Panel Protection and Power Down Sequencing
- Panel power Sequencing Control
- Supply Voltage 2.25-2.75V
- 64-pin LQFP Package (10 x 10 x 1.4mm)

1.6.5 VT1211 Super I/O

The VT1211 is a full function Super I/O chip that provides the most commonly used legacy Super I/O functionality plus the latest Hardware monitor initiatives. The device uses an LPC interface that complies with "LPC Interface Specification Revision 1.0".

The VT1211 contains a Floppy Disk Controller, an IEEE-1284 Parallel Port interface, two 16C550-UART-based serial port interfaces, a VFIR (Very Fast IR) Controller, a game port which supports 2 joysticks, a MIDI interface and a 4M Flash-ROM interface. The integrated Hardware Monitor Controller controls the speed of 2 fans, monitors 2 fan tachometers and has a Pentium II thermal diode and 5 Universal analog inputs for measuring voltage or temperature (by connecting external thermistors). The VT1211 meets the "Microsoft PC98 & PC99 system design guide" requirements and is ACPI ready. The device requires a 48 MHz clock input and operates at 3.3V power supply.

The VT1211 consists of following logical devices. One high-performance 2.88MB floppy disk controller, with digital data separator, which supports one 360K / 720K / 1.2M / 1.44M / 2.88M floppy disk drive; One multi-mode high-performance parallel port featuring support for bi-directional Standard Parallel Port (SPP), Enhanced Parallel Port (EPP v1.7 and v1.9) and IEEE1284 compliant Extended Capabilities Port (ECP) protocols; Two 16C550 standard compatible enhanced UARTs perform asynchronous communication; One VFIR interface compliant with IrDA; One MIDI interface; One game port with built-in 558 and buffer chips to support direct connect of 2 joysticks; One Hardware Monitor; and Seven GPIO ports (56 GPIO pins).

A hardware monitor engine is built in to monitor system health. An enhanced 8 bit ADC is built inside. This is exploited to simultaneously monitor 8 analog voltages or thermal inputs. The thermal inputs can be defined independently as thermistor or PentiumTM II thermal diode. Besides the ADC, the Hardware Monitor subsystem is also equipped with one chassis-open detection and 5 VID inputs for PentiumTM II Vcore identification. All logical devices can be individually enabled or disabled via software configuration registers.

1.6.6 Ethernet

1.6.6.1 Realtek RTL8111B Ethernet Controller

The Realtek RTL8111 Gigabit Ethernet controller combines a triple-speed IEEE 802.3 compliant Media Access Controller (MAC) with a triple-speed Ethernet transceiver, PCI Express bus controller, and embedded memory. With state-of-the-art DSP technology and mixed-mode signal technology, it offers high-speed transmission over CAT 5 UTP cable or CAT 3 UTP (10Mbps only) cable. Functions such as Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction are implemented to provide robust transmission and reception capability at high speeds.

The device supports the PCI Express 1.0a bus interface for host communications with power management and is compliant with the IEEE 802.3u specification for 10/100Mbps Ethernet and the IEEE 802.3ab specification for 1000Mbps Ethernet. It also supports an auxiliary power auto-detect function, and will auto-configure related bits of the PCI power management registers in PCI configuration space.

Advanced Configuration Power management Interface (ACPI)--power management for modern operating systems that are capable of Operating System-directed Power Management (OSPM)—is also supported to achieve the most efficient power management possible. PCI Message Signaled Interrupt (MSI) is also supported.

In addition to the ACPI feature, remote wake-up (including AMD Magic Packet[™], Re-LinkOk, and Microsoft[®] Wake-up frame) is supported in both ACPI and APM (Advanced Power Management) environments. To support WOL from a deep power down state (e.g., D3cold, i.e. main power is off and only auxiliary exists), the auxiliary power source must be able to provide the needed power for the RTL8111.

The RTL8111 is fully compliant with Microsoft® NDIS5 (IP, TCP, UDP) Checksum and Segmentation Task-offload features, and supports IEEE 802 IP Layer 2 priority encoding and 802.1Q Virtual bridged Local Area Network (VLAN). The above features contribute to lowering CPU utilization, especially benefiting performance when in operation on a network server.

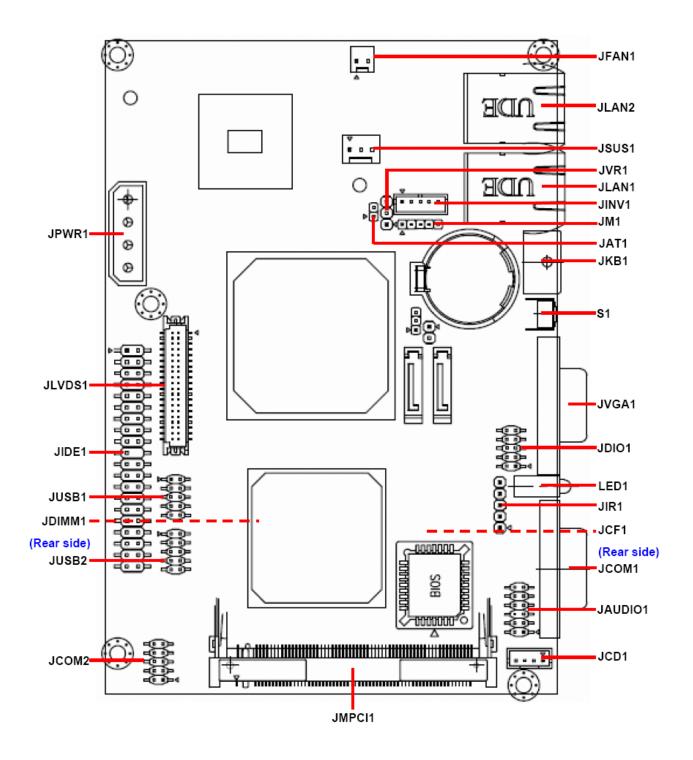
The device features next-generation PCI Express interconnect technology. PCI Express is a high-bandwidth, low pin count, serial, interconnect technology that offers significant improvements in performance over conventional PCI and also maintains software compatibility with existing PCI infrastructure.

1.6.7 Compact Flash Interface

A Compact Flash type II connector is connected to the secondary IDE controller. The Compact Flash storage card is IDE compatible. It is an ideal replacement for standard IDE hard drives. The solid-state design offers no seek errors even under extreme shock and vibration conditions. The Compact Flash storage card is extremely small and highly suitable for rugged environments, thus providing an excellent solution for mobile applications with space limitations. It is fully compatible with all consumer applications designed for data storage PC card, PDA, and Smart Cellular Phones, allowing simple use for the end user. The Compact Flash storage card is O/S independent, thus offering an optimal solution for embedded systems operating in non-standard computing environments. The Compact Flash storage card is IDE compatible and offers various capacities.

2. Hardware Configuration

2.1 Product Overview



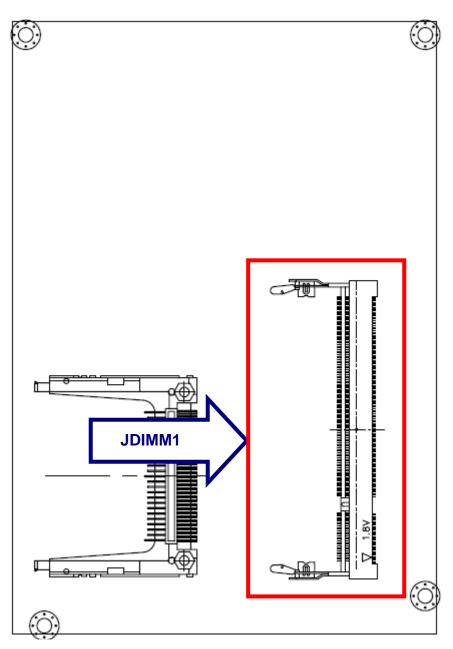
2.2 Installation Procedure

This chapter explains you the instructions of how to setup your system.

- 1. Turn off the power supply.
- 2. Insert the DIMM module (be careful with the orientation).
- 3. Insert all external cables for hard disk, floppy, keyboard, mouse, USB etc. except for flat panel. A CRT monitor must be connected in order to change CMOS settings to support flat panel.
- 4. Connect power supply to the board via the ATXPWR.
- 5. Turn on the power.
- 6. Enter the BIOS setup by pressing the delete key during boot up. Use the "LOAD BIOS DEFAULTS" feature. The *Integrated Peripheral Setup* and the *Standard CMOS Setup* Window must be entered and configured correctly to match the particular system configuration.
- 7. If TFT panel display is to be utilized, make sure the panel voltage is correctly set before connecting the display cable and turning on the power.

2.2.1 Main Memory

ECM-3711 series provides one 200-pin DIMM sockets to support DDR2 SDRAM. The total maximum memory size is 1GB.

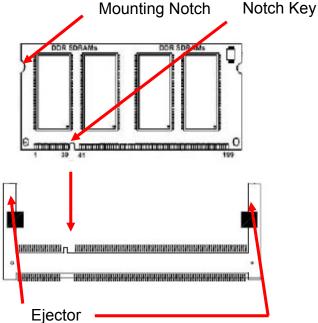


(Rear Side)



Make sure to unplug the power supply before adding or removing DIMMs or other system components. Failure to do so may cause severe damage to both the board and the components.

- Locate the DIMM socket on the board.
- Hold two edges of the DIMM module carefully. Keep away of touching its connectors.
- Align the notch key on the module with the rib on the slot.
- Firmly press the modules into the socket automatically snaps into the mounting notch.
 Do not force the DIMM module in with extra force as the DIMM module only fit in one direction.



200-pin DDR2 DIMM

• To remove the DIMM modules, push the two ejector tabs on the slot outward simultaneously, and then pull out the DIMM module.

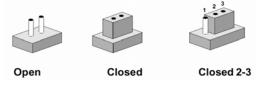


- **Note:** (1) Please do not change any DDR2 SDRAM parameter in BIOS setup to increase your system's performance without acquiring technical information in advance.
 - (2) Static electricity can damage the electronic components of the computer or optional boards. Before starting these procedures, ensure that you are discharged of static electricity by touching a grounded metal object briefly.

2.3 Jumper and Connector List

You can configure your board to match the needs of your application by setting jumpers. A jumper is the simplest kind of electric switch.

It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To "close" a jumper you connect the pins with the clip. To "open" a jumper you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2, and 3. In this case, you would connect either two pins.



The jumper settings are schematically depicted in this manual as follows:

0 0		1 2 3 O
Open	Closed	Closed 2-3

A pair of needle-nose pliers may be helpful when working with jumpers.

Connectors on the board are linked to external devices such as hard disk drives, a keyboard, or floppy drives. In addition, the board has a number of jumpers that allow you to configure your system to suit your application.

If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

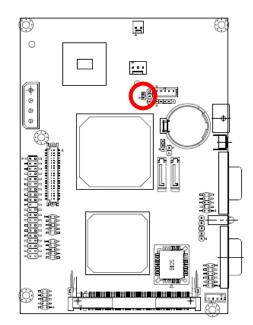
The following tables list the function of each of the board's jumpers and connectors.

Jumpers		
Label	Function	Note
JAT1	AT/ATX Power Select	3 x 1 header, pitch 2.0mm
JCMOS1	Clear CMOS	3 x 1 header, pitch 2.0mm

Connectors		
Label	Function	Note
JAUDIO1	Audio connector	5 x 2 header, pitch 2.0mm
JCD1	CD-ROM audio input connector	4 x 1 wafer, pitch 2.0mm
JCF1	Compact Flash connector	
JCOM1	Serial port 1 connector	D-sub 9-pin, male
JCOM2	Serial port 2 connector	5 x 2 header, pitch 2.0mm
JDIMM1	200-pin DDR2 SODIMM socket	
JDIO1	General purpose I/O connector	5 x 2 header, pitch 2.0mm
JFAN1	CPU fan connector	2 x 1 wafer, pitch 2.54mm
JIDE1	Primary IDE connector	20 x 2 header, pitch 2.54mm
JINV1	LCD inverter connector	5 x 1 wafer, pitch 2.0mm
JIR1	IrDA connector	5 x 1 header, pitch 2.54mm
JKB1	PS/2 keyboard & mouse connector	6-pin Mini-DIN
JLAN1	RJ-45 Ethernet 1	
JLAN2	RJ-45 Ethernet 2	
JLVDS1	LVDS connector	HIROSE DF13-40DP-1.25V
JM1	Load Port (for Firmware updating only)	5 x 1 header, pitch 2.0mm
JMPCI1	Mini PCI connector	
JPS1	ATX power switch connector	2 x 1 header, pitch 2.54mm
JPWR1	Power connector	
JSATA1	Serial ATA connector 1	
JSATA2	Serial ATA connector 2	
JSUS1	Singer power connector	3 x 1 header, pitch 2.54mm
JUSB1	USB connector 0 & 1	5 x 2 header, pitch 2.0mm
JUSB2	USB connector 2 & 3	5 x 2 header, pitch 2.0mm
JVGA1	VGA Port	D-sub 15-pin, Female
JVR1	LCD backlight brightness adjustment	3 x 1 header, pitch 2.54mm
LED1	Power & HDD indicator	
S1	Reset button	

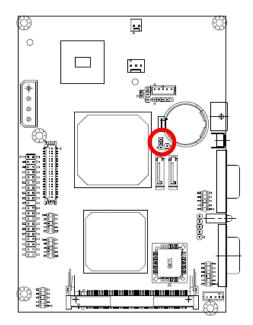
2.4 Setting Jumpers & Connectors

2.4.1 AT/ATX Power Select (JAT1)



* Default

2.4.2 Clear CMOS (JCMOS1)



* Default

Protect*

AT*

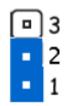
2

ATX

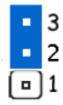
a |2

o |1

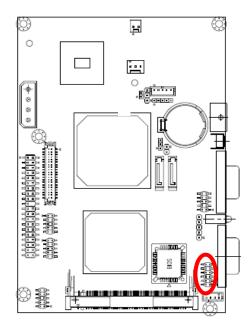
1

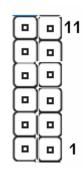


Clear CMOS



2.4.3 Audio connector (JAUDIO1)





Signal	PIN	PIN	Signal
GND	12	11	SPDIF OUT
NC	10	9	NC
Mic Bias	8	7	Mic-in
LIN_R	6	5	LIN_L
GND	4	3	GND
LINEOUT _R	2	1	LINEOUT_L

2.4.3.1 Signal Description – Audio Connecter (JAUDIO1)

Signal	Signal Description		
LINEOUT L/R	Left and right speaker output. These are the speaker outputs directly from the		
LINEOUTL/K	speaker amplifier.		
Mic-in	The MIC signal is used for microphone input. This input is fed to the left		
microphone channel.			
Line-In L/R	Left and right line in signals.		
LN L/R	Left and right line out signals. Both signals are capacitor coupled and should have		
	GND as return.		
SPDIF OUT PCM Non-Audio Sony/Philips Digital I/F Output (Internal pulled high).			
Mic Bias	Mic Bias provides 3.3V supplied through 3.2K Ω with capacitive decoupling to		
IVIIC DIdo	GND. This signal may be used for bias of some microphone types.		

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2.4.4 CD-ROM Audio Input Connector (JCD1)

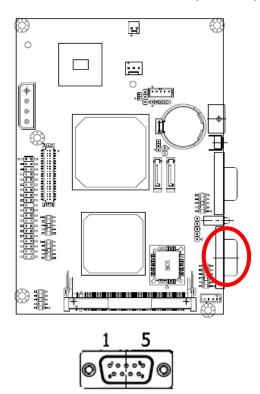
4	<u>-</u> 1
Signal	PIN
CD_L	4
GND	3
CD_R	2
GND	1

ה

2.4.4.1 Signal Description – CD-ROM Audio Input Connecter (JCD1)

Signal	Signal Description
CD_R	Right CD-IN signal
CD_L	Left CD-IN signal.

2.4.5 Serial Port 1 Connector (JCOM1)

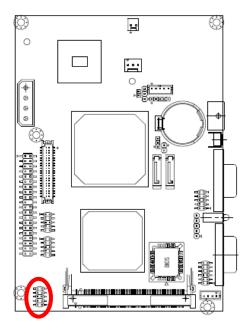


Signal	PIN	PIN	Signal
GND	5		
		9	RI
DTR	4		
		8	CTS
TxD	3		
		7	RTS
RxD	2		
		6	DSR
DCD	1		

Signal	Signal Description
	Serial output. This signal sends serial data to the communication link. The signal is
TxD	set to a marking state on hardware reset when the transmitter is empty or when
	loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTD	Data Terminal Ready. This signal indicates to the modem or data set that the
DTR	on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to
Dok	establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board
RIS	UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to
013	exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected
DCD	the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone
	ringing signal.

2.4.5.1 Signal Description – Serial Port 1 Connecter (JCOM1)

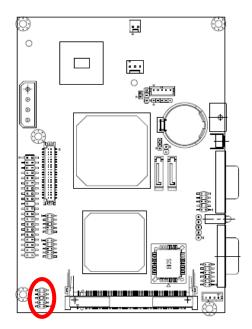
2.4.6 Serial Port Connector in RS-232 Mode (JCOM2)

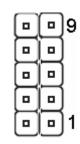




Signal	PIN	PIN	Signal
GND	10	9	RI
CTS	8	7	RTS
DSR	6	5	GND
DRT	4	3	TxD
RxD	2	1	DCD

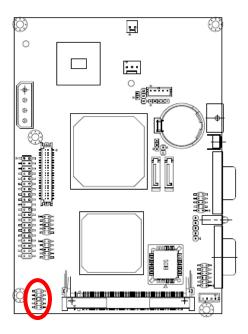
2.4.7 Serial Port Connector in RS-422 Mode (JCOM2)

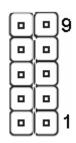




Signal	PIN	PIN	Signal
GND	10	9	GND
RxD-	8	7	NC
TxD+	6	5	GND
NC	4	3	NC
RxD+	2	1	TxD-

2.4.8 Serial Port Connector in RS-485 Mode (JCOM2)





Signal	PIN	PIN	Signal
GND	10	9	GND
NC	8	7	NC
DATA+	6	5	GND
NC	4	3	NC
NC	2	1	DATA-

Signal	Signal Description
TxD	Serial output. This signal sends serial data to the communication link. The signal is set to a marking state on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RxD	Serial input. This signal receives serial data from the communication link.
DTR	Data Terminal Ready. This signal indicates to the modem or data set that the on-board UART is ready to establish a communication link.
DSR	Data Set Ready. This signal indicates that the modem or data set is ready to establish a communication link.
RTS	Request To Send. This signal indicates to the modem or data set that the on-board UART is ready to exchange data.
CTS	Clear To Send. This signal indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect. This signal indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator. This signal indicates that the modem has received a telephone ringing signal.
TxD+/-	Serial output. This differential signal pair sends serial data to the communication link. Data is transferred from Serial Port 2 Transmit Buffer Register to the communication link, if the RTS register of the Serial Port 2 is set to LOW.
RxD+/-	Serial input. This differential signal pair receives serial data from the communication link. Received data is available in Serial Port 2 Receiver Buffer Register.
DATA+/-	This differential signal pair sends and receives serial data to the communication link. The mode of this differential signal pair is controlled through the RTS register of Serial Port 2. Set the RTS register of the Serial Port 2 to LOW for transmitting, HIGH for receiving.

2.4.8.1 Signal Description – Serial Port 2 Connecter (JCOM2)



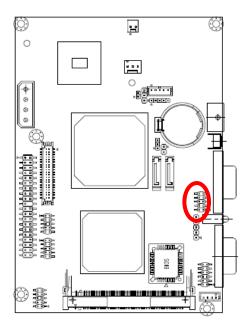
Do not select a mode different from the one used by the connected peripheral, as this may damage CPU board and/or peripheral.

The transmitter drivers in the port are short circuit protected by a thermal protection circuit. The circuit disables the drivers when the die temperature reaches 150 $^{\circ}$ C.

RS-422 mode is typically used in point to point communication. Data and control signal pairs should be terminated in the receiver end with a resistor matching the cable impedance (typical 100-120 Ω). The resistors could be placed in the connector housing.

RS-485 mode is typically used in multi drop applications, where more than 2 units are communicating. The data and control signal pairs should be terminated in each end of the communication line with a resistor matching the cable impedance (typical 100-120 Ω). Stubs to substations should be avoided.

2.4.9 General Purpose I/O Connector (JDIO1)



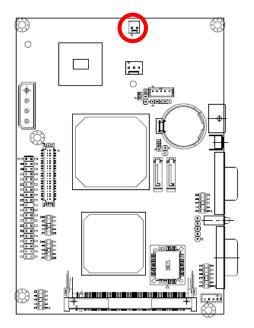
			9
	▣		
	▣	▣	
	▣	▣	
		▣	1

Signal	PIN	PIN	Signal
GND	10	9	+5V
GP17	8	7	GP13
GP16	6	5	GP12
GP15	4	3	GP11
GP14	2	1	GP10

2.4.9.1 Signal Description – General Purpose I/O Connecter (JDIO1)

Signal	Signal Description	
GP [10:17]	Digital Input/Output Data Bit 0 to Bit 8	

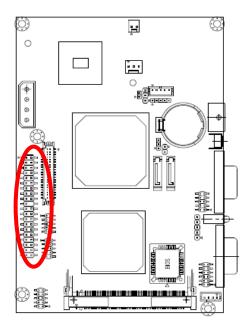
2.4.10 System Fan Connector (JFAN1)

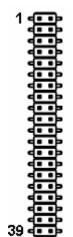




Signal	PIN
GND	1
VDD	2

2.4.11 Primary IDE Connector (JIDE1)

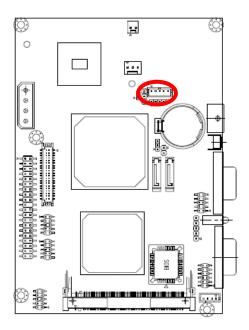




Signal	PIN	PIN	Signal
RESET#	1	2	GND
PDD7	3	4	PDD8
PDD6	5	6	PDD9
PDD5	7	8	PDD10
PDD4	9	10	PDD11
PDD3	11	12	PDD12
PDD2	13	14	PDD13
PDD1	15	16	PDD14
PDD0	17	18	PDD15
GND	19	20	NC
PDREQ	21	22	GND
PDIOW#	23	24	GND
PDIOR#	25	26	GND
PIORDY	27	28	GND
PDDACK#	29	30	GND
IRQ14	31	32	NC
PDA1	33	34	NC
PDA0	35	36	PDA2
PDCS1#	37	38	PDCS3#
IDEACTP#	39	40	GND

Signal	Signal Description
PDA [2:0]	IDE Address Bits. These address bits are used to access a register or data port in
	a device on the IDE bus.
DCS1#, DCS3#	IDE Chip Selects. The chip select signals are used to select the command block
	registers in an IDE device. DCS1# selects the primary hard disk.
PDD [15:0]	IDE Data Lines. D [15:0] transfers data to/from the IDE devices.
PIOR#	IDE I/O Read. Signal is asserted on read accesses to the corresponding IDE port
	addresses.
PIOW#	IDE I/O Write. Each signal is asserted on write accesses to corresponding the IDE
	port addresses.
PIORDY	When deasserted, these signals extend the transfer cycle of any host register
	access when the device is not ready to respond to the data transfer request.
RESET#	IDE Reset. This signal resets all the devices that are attached to the IDE
	interface.
PIRQ14	Interrupt line from hard disk. Connected directly to PC-AT bus.
PDREQ	The DREQ is used to request a DMA transfer from the South Bridge. The
	direction of the transfers is determined by the IOR#/IOW# signals.
PDACK#	DMA Acknowledge. The DACK# acknowledges the DREQ request to initiate DMA
	transfers.
PDACT#	Signal from hard disk indicating hard disk activity. The signal level depends on the
	hard disk type, normally active low. The signal is routed directly to the LED1.

2.4.11.1 Signal Description – Primary IDE Connector (JIDE1)



1	5 • • •
Signal	PIN
+12V	1
GND	2
ENBKL	3
VR	4
+5V	5



Note:

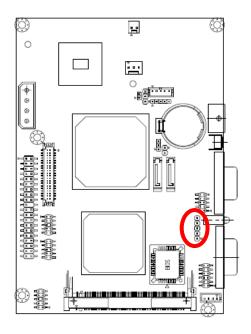
For inverters with adjustable Backlight function, it is possible to control the LCD brightness through the VR signal controlled by **JVR1**. Please see the **JVR1** section for detailed circuitry information.

2.4.12.1 Signal Description – LCD Inverter Connector (JINV1)

Signal	Signal Description
VR	Vadj = 0.75V ~ 4.25V (Recommended: 4.7KΩ, >1/16W)
ENBKL	LCD backlight ON/OFF control signal

2.4.12 LCD Inverter Connector (JINV1)

2.4.13 IrDA Connector (JIR1)



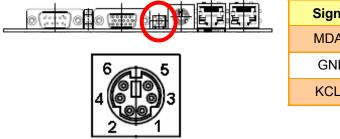


Signal	PIN
IRTX	5
GND	4
IRRX	3
NC	2
+5V	1

2.4.13.1 Signal Description – IrDA Connector (JIR1)

Signal	Signal Description
IRRX	Infrared Receiver input
IRTX	Infrared Transmitter output

2.4.14 PS/2 Keyboard & Mouse Connector (JKB1)

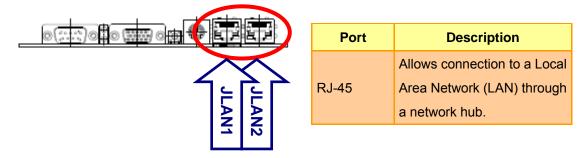


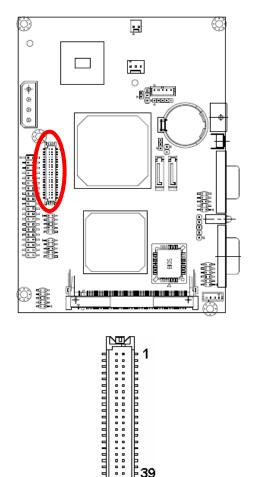
Signal	PIN	PIN	Signal
MDAT	6	5	KDAT
GND	4	3	+5V
KCLK	2	1	MCLK

2.4.14.1 Signal Description – PS/2 Keyboard & Mouse Connector (JKB1)

Signal	Signal Description
KCLK	Bi-directional clock signal used to strobe data/commands from/to the PC-AT keyboard.
	Bi-directional serial data line used to transfer data from or commands to the PC-AT
KDAT	keyboard.
MCLK	Bi-directional clock signal used to strobe data/commands from/to the PS/2 mouse.
MDAT	Bi-directional serial data line used to transfer data from or commands to the PS/2 mouse.

2.4.15 RJ-45 Ethernet (JLAN1, JLAN2)





2.4.16 LVDS Connector (JLVDS1)

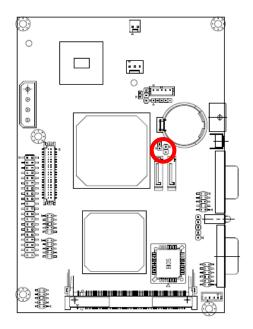
Signal	PIN	PIN	Signal
+5V	2	1	+3.3V
+5V	4	3	+3.3V
I ² C_DAT	6	5	I ² C_CLK
GND	8	7	GND
Txout0	10	9	Txout1
Txout0#	12	11	Txout1#
GND	14	13	GND
Txout2	16	15	Txout3
Txout2#	18	17	Txout3#
GND	20	19	GND
E_Txout0	22	21	E_Txout1
E_Txout0#	24	23	E_Txout1#
GND	26	25	GND
E_Txout2	28	27	E_Txout3
E_Txout2#	30	29	E_Txout3
GND	32	31	GND
Txclk	34	33	E_Txclk
Txclk#	36	35	E_Txclk#
GND	38	37	GND
+12V	40	39	+12V

2.4.16.1 Signal Description – LVDS Connector (JLVDS1)

39

Signal	Description
I ² C_DAT, I ² C_CLK	I ² C interface for panel parameter EEPROM. This EERPOM is mounted on the LVDS receiver. The data in the EEPROM allows the EXT module to automatically set the proper timing parameters for a specific LCD panel.

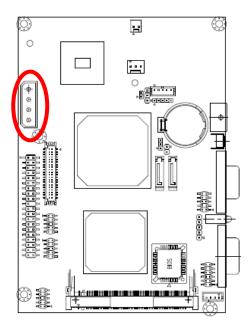
2.4.17 ATX Power Switch Connector (JPS1)

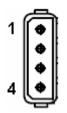




Signal	PIN
GND	2
PW_BN	1

2.4.18 Power Connector (JPWR1)





PIN	Signal
1	+12V
2	GND
3	GND
4	+5V

PIN

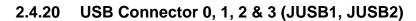
1

2

3

0 O) 0 2... • B Signal I PWR_ON J, +5V VCCSB 8f 0000 Note: The default sets 2-3 closed AAAAA for single power used. 0000

Single Power Select (JSUS1) 2.4.19



Signa
+5V
D1-/D3
D1+/D3
GND

1		
	▣	▣
	▣	▣
	▣	▫
9	▣	▣

Signal	PIN	PIN	Signal
+5V	1	2	GND
D1-/D3-	3	4	GND
D1+/D3+	5	6	D0+/D2+
GND	7	8	D0-/D2-
GND	9	10	+5V

2.4.20.1 Signal Description – USB Connector 0, 1, 2 & 3 Connector (JUSB1, JUSB2)

Signal	Signal Description
D0+/-, D2+/-	Differential bi-directional data signal for USB channel 0, 2. Clock is transmitted
DU+/-, D2+/-	along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.
D1+/-, D3+/-	Differential bi-directional data signal for USB channel 1, 3. Clock is transmitted
ט דין, שטדי-	along with the data using NRZI encoding. The signalling bit rate is up to 12 Mbs.

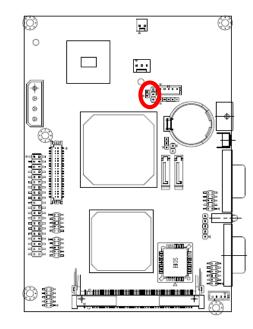
2.4.21 VGA Connector (JVGA1)



Signal	PIN			Signal
		6		GND
RED	1		11	NC
		7		GND
GREEN	2		12	DAT
		8		GND
BLUE	3		13	HSYNC
		9		VCC
NC	4		14	VSYNC
		10		GND
GND	5		15	DCK

2.4.21.1 Signal Description – VGA Connecter (JVGA1)

Signal	Signal Description
HSYNC	CRT horizontal synchronisation output.
VSYNC	CRT vertical synchronisation output.
DCK	Display Data Channel Clock. Used as clock signal to/from monitors with DDC interface.
DAT	Display Data Channel Data. Used as data signal to/from monitors with DDC interface.
RED	Analog output carrying the red colour signal to the CRT. For 75 $\mbox{$\Omega$}$ cable impedance.
GREEN	Analog output carrying the green colour signal to the CRT. For 75 $\mbox{$\Omega$}$ cable impedance.
BLUE	Analog output carrying the blue colour signal to the CRT. For 75 $\ensuremath{\Omega}$ cable impedance.



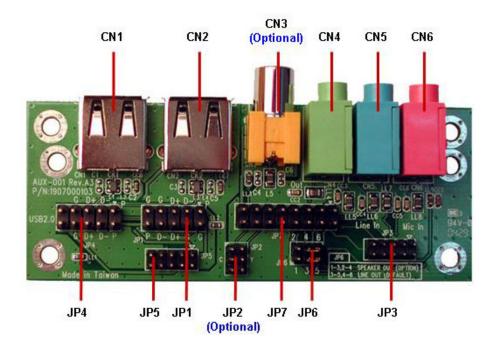
3 2 1 PIN Signal +5V 3 VR 2 GND 1 vcc JVR1 \bigcirc 3 JINV1 pin 4 \bigcirc 2 \bigcirc

Variation Resistor (Recommended: $4.7K\Omega$, >1/16W)

2.4.22 LCD Backlight Brightness Adjustment Connector (JVR1)

2.5 Audio / USB Daughter Board User's Guide

2.5.1 Jumper and Connector Layout



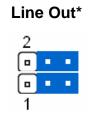
2.5.2 Jumper and Connector List

Jumpers		
Label	Function	Note
	Line out / Speaker out select (The speaker	1-3, 2-4 Speaker out
JP6	out function is only available in combine	3-5, 4-6 Line out (Default)
	used of main board)	

Connectors	5	
Label	Function	Note
CN1, CN2	USB 1.1/2.0 connector	
CN3	TV out connector (Optional)	RCA connector
CN4	Line out connector	Phone Jack
CN5	Line in connector	Phone Jack
CN6	Mic in connector	Phone Jack
JP1	2.54mm USB 1.1/2.0 connector 1	5 x 2 header, pitch 2.54mm
JP2	2.0mm Connector for S-Video (Optional)	3 x 2 header, pitch 2.0mm
JP3	Audio connector	5 x 2 header, pitch 2.0mm
JP4	2.54mm USB 1.1/2.0 connector 2	5 x 2 header, pitch 2.54mm
JP5	2.0mm USB 1.1/2.0 connector	5 x 2 header, pitch 2.0mm
JP7	TV / Audio connector	8 x 2 header, pitch 2.54mm

2.5.3 Setting Jumper and Connector

Line out / Speaker out Select (JP6)



Speaker Out



2.0mm Connector for S-Video Signal (JP2)

PIN

2

4

6

Signal

GND

Yout

GND

PIN

1

3

5

2.54mm USB 1.1/2.0 Connector 1 (JP1)

Signal	PIN	PIN	Signal
+5V	1	2	GND
D1-	3	4	GND
D1+	5	6	D2+
GND	7	8	D2-
GND	9	10	+5V

Note: \

Note: Wrong USB cable configuration with your USB devices might cause your USB devices damaged.

Audio Connector (JP3)

Signal	PIN	PIN	Signal
Line out R	1	2	Line out L
GND	3	4	GND
Line in R	5	6	Line in L
Mic In	7	8	Mic Bais
SPK R	9	10	SPK L

2.54mm USB 1.1/2.0 Connector 2 (JP4)

Signal

GND

Cout

GND

Signal	PIN	PIN	Signal
+5V	1	2	+5V
D1-	3	4	D2-
D1+	5	6	D2+
GND	7	8	GND
NC	9	10	NC

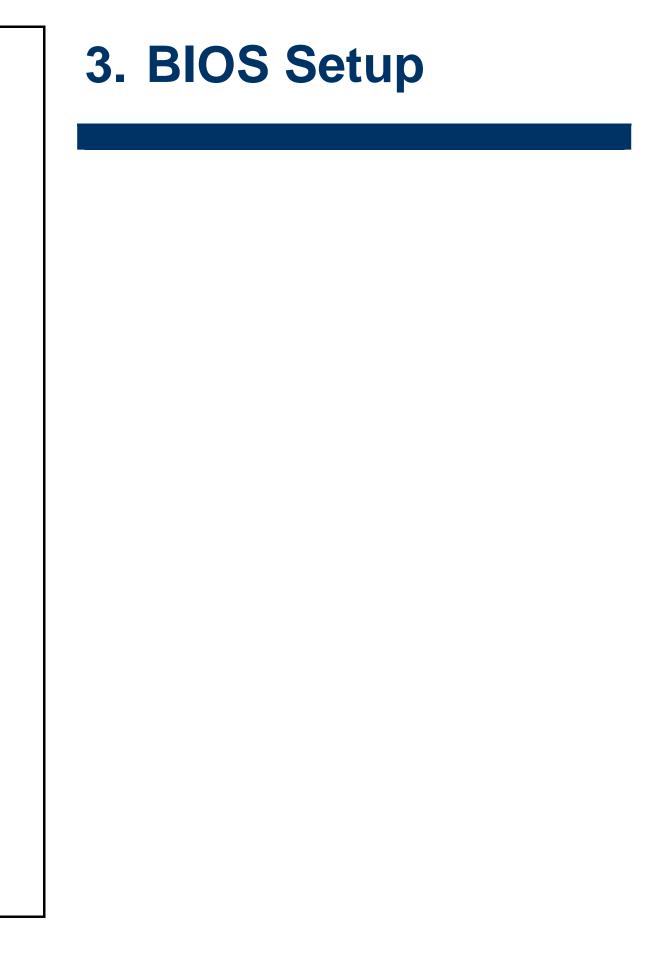
2.0mm USB 1.1/2.0 Connector (JP5)

Signal	PIN	PIN	Signal
+5V	1	2	GND
D1-	3	4	GND
D1+	5	6	D2+
GND	7	8	D2-
GND	9	10	+5V

TV / Audio Connector (JP7)

Signal	PIN	PIN	Signal
Mic In	1	2	Mic Bais
GND	3	4	GND
Line out L	5	6	Line out R
SPK L	7	8	SPK R
Line in L	9	10	Line in R
GND	11	12	Yout
TVGND	13	14	Cout
TVGND	15	16	COMP

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3.1 Starting Setup

The AwardBIOS[™] is immediately activated when you first power on the computer. The BIOS reads the system information contained in the CMOS and begins the process of checking out the system and configuring it. When it finishes, the BIOS will seek an operating system on one of the disks and then launch and turn control over to the operating system.

While the BIOS is in control, the Setup program can be activated in one of two ways:

By pressing immediately after switching the system on, or

By pressing the key when the following message appears briefly at the bottom of the screen during the POST (Power On Self Test).

Press DEL to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system to try again by turning it OFF then ON or pressing the "RESET" button on the system case. You may also restart by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys. If you do not press the keys at the correct time and the system does not boot, an error message will be displayed and you will again be asked to.

Press F1 to Continue, DEL to enter SETUP

3.2 Using Setup

In general, you use the arrow keys to highlight items, press <Enter> to select, use the PageUp and PageDown keys to change entries, press <F1> for help and press <Esc> to quit. The following table provides more detail about how to navigate in the Setup program using the keyboard.

Button	Description
1	Move to previous item
\downarrow	Move to next item
\downarrow	Move to the item in the left hand
\rightarrow	Move to the item in the right hand
Esc key	Main Menu Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu Exit current page and return to Main Menu
PgUp key	Increase the numeric value or make changes
PgDn key	Decrease the numeric value or make changes
+ key	Increase the numeric value or make changes
- key	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
(Shift) F2 key	Change color from total 16 colors. F2 to select color forward, (Shift) F2 to select color backward
F3 key	Calendar, only for Status Page Setup Menu
F4 key	Reserved
F5 key	Restore the previous CMOS value from CMOS, only for Option Page Setup Menu
F6 key	Load the default CMOS value from BIOS default table, only for Option Page Setup Menu
F7 key	Load the default
F8 key	Reserved
F9 key	Reserved
F10 key	Save all the CMOS changes, only for Main Menu

• Navigating Through The Menu Bar

Use the left and right arrow keys to choose the menu you want to be in.



Note: Some of the navigation keys differ from one screen to another.

• To Display a Sub Menu

Use the arrow keys to move the cursor to the sub menu you want. Then press <Enter>. A " \geq " pointer marks all sub menus.

3.3 Getting Help

Press F1 to pop up a small help window that describes the appropriate keys to use and the possible selections for the highlighted item. To exit the Help Window press <Esc> or the F1 key again.

3.4 In Case of Problems

If, after making and saving system changes with Setup, you discover that your computer no longer is able to boot, the AwardBIOS[™] supports an override to the CMOS settings which resets your system to its defaults.

The best advice is to only alter settings which you thoroughly understand. To this end, we strongly recommend that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your systems manufacturer to provide the absolute maximum performance and reliability. Even a seemingly small change to the chipset setup has the potential for causing you to use the override.

3.5 Main Menu

Once you enter the AwardBIOS[™] CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

Note that a brief description of each highlighted selection appears at the bottom of the screen.

Phoenix - AwardBIOS	CMOS Setup Utility	
Standard CMOS Features	► Frequency/Voltage Control	
Advanced BIOS Features	Load Fail-Safe Defaults	
Advanced Chipset Features	Load Optimized Defaults	
Integrated Peripherals	Set Supervisor Password	
▶ Power Management Setup	Set User Password	
PnP/PCI Configurations	Save & Exit Setup	
► PC Health Status	Exit Without Saving	
Esc : Quit F9 : Menu in BIOS ↑↓→→ : Select Item F10 : Save & Exit Setup		
Time, Date, Hard Disk Type		



Note: The BIOS setup screens shown in this chapter are for reference purposes only, and may not exactly match what you see on your screen. Visit the Evalue website (<u>www.evalue-tech.com</u>) to download the latest product and BIOS information.

3.5.1 Standard CMOS Features

The items in Standard CMOS Setup Menu are divided into few categories. Each category includes no, one or more than one setup items. Use the arrow keys to highlight the item and then use the <PgUp> or <PgDn> keys to select the value you want in each item.

Phoenix - AwardBIOS CMOS Setup Utility Standard CMOS Features		
Date (mm:dd:yy) Time (hh:mm:ss)	Tue, <mark>Jul</mark> 20 1999 10 : 24 : 31	Item Help
► IDE Channel Ø Master	10.24.31	Menu Level 🕞 🕨
 IDE Channel Ø Master IDE Channel Ø Slave IDE Channel 1 Master IDE Channel 1 Slave 		Change the day, month, year and century
Video Halt On	[EGA/VGA] [All , But Keyboard]	
Base Memory Extended Memory Total Memory	636K 64512K 65536K	
↑↓→+:Move Enter:Select F5: Previous Values		ESC:Exit F1:General Help F7: Optimized Defaults

3.5.1.1 Main Menu Selection

This reference table shows the selections that you may make on the Main Menu.

ltem	Options	Description
Date	MM DD YYYY	Set the system date. Note that the 'Day' automatically changes when you set the date
Time	HH : MM : SS	Set the system time
IDE Channel 0 Master IDE Channel 0 Slave IDE Channel 1 Master IDE Channel 1 Slave	Options are in 3.5.1.2	Press <enter> to enter the sub menu of detailed options</enter>
Video	EGA/VGA CGA 40 CGA 80 MONO	Select the default video device
Halt On	All Errors No Errors All, but Keyboard	Select the situation in which you want the BIOS to stop the POST process and notify you

3.5.1.2 IDE Adapter Setup

The IDE adapters control the hard disk drive. Use a separate sub menu to configure each hard disk drive. The below Figure will shows the IDE primary master sub menu.

ltem	Options	Description
IDE HDD Auto-detection	Press Enter	Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.
IDE Channel 0 Master IDE Channel 0 Slave, IDE Channel 1 Master, IDE Channel 1 Slave	None Auto Manual	Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !
Access Mode	CHS LBA Large Auto	Choose the access mode for this hard disk
The following op	tions are selectable only if the	'IDE Channel' item is set to 'Manual'
Cylinder	Min = 0 Max = 65535	Set the number of cylinders for this hard disk.
Head	Min = 0 Max = 255	Set the number of read/write heads
Precomp	Min = 0 Max = 65535	**** Warning : Setting a value of 65535 means no hard disk
Landing zone	Min = 0 Max = 65535	***
Sector	Min = 0 Max = 255	Number of sectors per track

3.5.2 Advanced BIOS Features

This section allows you to configure your system for basic operation. You have the opportunity to select the system's default speed, boot-up sequence, keyboard operation, shadowing and security.



3.5.2.1 CPU Feature

This item allows you to select the CPU feature.

Phoenix - AwardBIOS CMOS Setup Utility CPU Feature			
Delay Prior to Therma		Item Help	
Thermal Management × TM2 Bus Ratio × TM2 Bus VID Execute Disable Bit	[Thermal Monitor 1] 0 X 0.700V [Enabled]	Menu Level 🔸	
↑↓→+:Move Enter:Select F5: Previous Values	+/-/PU/PD:Value F10:Save F6: Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults	

ltem	Option	Description
	4 Min	
Dolov Brier to Thormal	8 Min	
Delay Prior to Thermal	16 Min	
	32 Min	
Thermal Management	Thermal Monitor 1	
merma Management	Thermal Monitior 2	
Execute Disable Bit	Enabled	
	Disabled	

3.5.2.2 Hard Disk Boot Priority

This item allows you to select the Hard Disk device boot up priority.

1. Pri.Master:	Item Help
<pre>2. Pri.Slave : 3. Sec.Master: 4. Sec.Slave : 5. USBHDD0 : 6. USBHDD1 : 7. USBHDD2 : 8. Bootable Add-in Cards</pre>	Menu Level ►► Use <f> or <↓> to select a device , then press <+> to move it up , or <-> to move i down the list. Press <esc> to exit this menu.</esc></f>

Item	Description
Pri.Master	Boot up from IDE Primary Master Hard Disk
Pri.Slave	Boot up from IDE Primary Slave Hard Disk
Sec.Master	Boot up from IDE Secondary Master Hard Disk
Sec.Slave	Boot up from IDE Secondary Slave Hard Disk
USBHDD0	Boot up from First USB Hard Disk
USBHDD1	Boot up from Second USB Hard Disk
USBHDD2	Boot up from Thrid USB Hard Disk
Bootable Add-in Cards	Boot up from other Add-In Card Hard Disk Device.

3.5.2.3 Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep.

Item	Description
	Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.
	No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

3.5.2.4 CPU L1 & L2 Cache

This item allows you to enable the CPU L1 & L2 cache to speed up memory access. However, it depends on CPU design.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.5 CPU L3 Cache

This item allows you to enable the CPU L3 cache to speed up memory access.

Item	Description
Enabled	Enable cache
Disabled	Disable cache

3.5.2.6 CPU L2 Cache ECC Checking

This item allows you to enable the CPU external L2 cache use ECC checking method in memory access.

Item	Description	
Enabled	Enable ECC checking	
Disabled	Disable ECC checking	

3.5.2.7 Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it

is set to Enable, BIOS will shorten or skip some check items during POST.

Item	Description	
Enabled	Enable quick POST	
Disabled	Normal POST	

3.5.2.8 First / Second / Third Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items.

Item Des

Item	Description	
Floppy	Floppy Device	
LS120	LS120 Device	
Hard Disk	Hard Disk Device	
CDROM	CDROM Device	
ZIP100	ZIP-100 Device	
USB-FDD	USB Floppy Device	
USB-ZIP	USB ZIP Device	
USB-CDROM	USB CDROM Device	
LAN	Network Device	
Disabled Disabled any boot device		

3.5.2.9 Boot Other Device

This item allows you to enable the system to boot from other device.

Item	Description	
Enabled	Enable booting from other device	
Disabled	Disable booting from other device	

3.5.2.10 Boot Up NumLock Status

Select power on state for NumLock.

Item	Description
Off	Enable NumLock
On	Disable NumLock

3.5.2.11 Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

Item	Description	
Enabled	Enable typematic rate/delay setting	
Disabled	Disable typematic rate/delay setting	

3.5.2.12 Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

3.5.2.13 Typematic Rate (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

3.5.2.14 Security Option

Select whether the password is required every time the system boots or only when you enter setup.

Item	Description	
System	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.	
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.	



Note: To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

3.5.2.15 MPS Version Control For OS

This feature is only applicable to multiprocessor board as it specifies the version of the Multi-Processor Specification (MPS) that the board will use.

The choice: 1.4, 1.1.

3.5.2.16 OS Select for DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system.

Item	Description	
Non-OS2	Disable OS for over 64 MB DRAM	
OS2	Enable OS for over 64 MB DRAM	

3.5.2.17 Video BIOS Shadow

To allow copying Video BIOS into shadow RAM to improve video performance.

Item	Description	
Enable	Copy Video BIOS into shadow RAM	
Disable	Do not copy Video BIOS into shadow RAM	

3.5.2.18 Full Screen LOGO Show

If the BIOS had the full screen logo in it, this item could allow enable/ disable the full screen logo show on display.

Item	Description	
Enable	Enable full screen logo show	
Disable	Disable full screen logo show	

3.5.2.19 Small Logo (EPA) Show

This item allows you enabled/disabled the small EPA logo show on screen at the POST step.

Item	Description	
Enabled	EPA Logo show is enabled	
Disabled	EPA Logo show is disabled	

3.5.3 Advanced Chipset Features

This section allows you to configure the system based on the specific features of the installed chipset. This chipset manages bus speeds and access to system memory resources, such as DRAM and the external cache. It also coordinates communications between the conventional ISA bus and the PCI bus. It must be stated that these items should never need to be altered. The default settings have been chosen because they provide the best operating conditions for your system. The only time you might consider making any changes would be if you discovered that data was being lost while using your system.

The first chipset settings deal with CPU access to dynamic random access memory (DRAM). The default timings have been carefully chosen and should only be altered if data is being lost. Such a scenario might well occur if your system had mixed speed DRAM chips installed so that greater delays may be required to preserve the integrity of the data held in the slower memory chips.

Phoenix - AwardBIOS CMOS Setup Utility Advanced Chipset Features			
DRAM Clock/Drive Control	[Press Enter]	Item Help	
 ▶ AGP & P2P Bridge Control ▶ CPU & PCI Bus Control Memory Hole System BIOS Cacheable Video RAM Cacheable Init Display First 	[Press Enter] [Press Enter] [Disabled] [Enabled] [Disabled] [PCI Slot]	Menu Level 🕨	
	/PU/PD:Value F10:Save : Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults	

3.5.3.1 DRAM Clock/Drive Control

This section can set the DRAM clock/driver timing.

Item	Options	Description
DRAM Clock	By SPD 100NHz 133 MHz 166 MHz 200 MHz 266 MHz	Set the memory bus frequency to operate at various values for the proper memory clock setting
DRAM Timing	Manual Auto By SPD Turbo Ultra	Set the memory timings for the said timings or DRAM Cycle Lengths of 2 or 2.5.
SDRAM CAS Latency (DDR/DDR2)	1.5 / 2 2 / 3 2.5 / 4 3 / 5	This controls the time dealy passing before the SDRAM starts to carry out a read command after receiving it.
Bank Interleave	Diabled 2 Bank 4 Bank 8 Bank	Enables to set the interleave mode of the SDRM interface which allows banks of SDRAM to alternate their refresh and access cycles.
Precharge to Active(Trp)	2T 3T 4T 5T	This item sets the length of time taking to precharge a row in the memory module before a row being active and appears only when DRAM timing is set at Manual . Longer values are safer but probably not acting the best performance.
Active to Precharge(Tras)	5T, 6T, 7T, 8T 9T, 10T, 11T, 12T 13T, 14T, 15T, 16T 17T, 18T, 19T, 20T	This item sets the length of time that a row staying active fore precharging and appears only when DRAM timing is set at Manual . Longer values are safer but probably not acting the best performance.
Active to CMD(Trcd)	8T, 9T, 10T, 11T, 12T, 13T, 14T, 15T, 16T, 17T, 18T, 19T, 20T, 21T, 22T, 23T, 24T, 25T, 26T	This timing controls the length of the delay between when a memory bank is activated to when a read/write command is sent to that bank.
REF to ACT/REF to REF(Trfc)	12T 13T 14T 15T	Set the REF to ACT/REF to REF timing. This field appears when DRAM Timing is set at Manual .
ACT(0) to ACT(1) (TRRD)	2T 3T 4T 5T	Set the minimum time interval between successive ACTIVE commands to the different banks. This field appears when DRAM Timing is set at Manual .
Read to Precharge (Trtp)	2T 3T	Use this option to select Read to Precharge (Trtp) to set the timing by dram SPD.
Write to Read CMD (Twtr)	2T / 3T 1T / 2T	Use this option to select Write to Read CMD (Twtr) to set the timing by dram SPD.
Write Recovery Time (Twr)	2T 3T 4T 5T	Use this option to select Write Recovery Time (Twr) to set the timing by dram SPD.
DRAM Command Rate	2T Command 1T Command	Allows to set the DRAM Command Rate.
RDSAIT mode	Manual Auto	
RDSAIT selection	3	Key in a HEX number (Min = 0000, Max = 003F)

3.5.3.2 AGP & P2P Bridge Control

This item stores the onboard AGP and P2P function information. The reference table is as below.

Item	Options	Description
	32M,	Select the size of Accelerated Graphics Port
	64M,	(AGP) aperture. The aperture is a portion of the
	128M,	PCI memory address range dedicated for
AGP Aperture Size	256M,	graphics memory address space. Host cycles
	512M,	that hit the aperture range are forwarded to the
	1G [′]	AGP without any translation.
		This item allows you to select the AGP 2.0 mode
AGP 2.0 Mode	4X, 2X, 1X	to 4X,2X or 1X.
	Auto	This item allows you to select the AGP Driving
AGP Driving Control	Manual	Control to auto / disable Mode.
	Manual	This item allows you to set the AGP Driving
AGP Driving Value	00 ~ FF	value
	Enabled	This feature controls the AGP bus's Fast Write
AGP Fast Write	Disabled	capability. It accelerates memory write
		transactions from the chipset to the AGP device.
AGP Master 1 WS Write	Enabled	Enabled this item to increase AGP writing
	Disabled	
AGP Master 1 WS Read	Enabled	Enabled this item to increase AGP reading
	Disabled	-
		This option allows you to disable the AGP 3.0
		calibration cycle. This cycle ensures that the
ACB 2.0 Calibratian Cycla	Enabled	on-die termination impedance signal swing and
AGP 3.0 Calibration Cycle	Disabled	slew rate of the AGP signals are calibrated on a
		periodic basis to ensure signal integrity.
		It is recommended to keep this setting enabled.
	Disabled	Select the size of onboard video controller's
VGA Share Memory Size	2M, 4M, 8M	frame buffer. The buffer size shares from system
, ,	16M, 32M, 64M	memory unit.
	Enabled	This item allows you to select the Direct Frame
Direct Frame Buffer	Disabled	Buffer to enabled / disabled.
	AUTO, CRT, LCD,	
	TV, DVI, HDTV,	
	CRT+LCD, CRT+TV	
Select Display Device	CRT+DVI, CRT+HDTV	This item allows you to select display device.
	DVI+HTDV, LCD+DVI	
	TV+DVI	
	640x480 1x18B	
	800x600 1x18B	
	1024x768 1x18B	
	1280x768 1x18B	
	1280x1024 2x18B	
	1400x1050 2x18B	
	1600x1200 2x18B	
	1280x800 1x18B	
Panel Type	800x480 1x18B	This item allows you to select the panel type.
	1024x768 2x18B	
	1024x768 1x24B	
	1024x768 1x24B	
	1280x768 1x24B	
	1280x1024 2x24B	
	1280x1024 2x24B 1400x1050 2x24B	
Outport Dat	1280x1024 2x24B 1400x1050 2x24B 1600x1200 2x24B	This item allows you to apport the system to set
Outport Port Dithering	1280x1024 2x24B 1400x1050 2x24B	This item allows you to select the outport port. This item allows you to enable dithering.

3.5.3.3 CPU & PCI Bus Control

Phoenix - AwardBIOS CMOS Setup Utility CPU & PCI Bus Control					
PCI Master 0 WS Write				Item Help	
PCI Delay Transaction VLink mode selection VLink 8X Support DRDY_Timing	[Enabled] [By Auto] [Enabled] [Default]		Menu Le	vel ►	
1↓→+:Move Enter:Select	+/-/PU/PD:Value	F10:Save	ESC:Exit	F1:General	Help

F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

Item	Options	Description
PCI Master 0 WS Write	Enabled Disabled	To write PCI bus while zero wait state is executed.
PCI Delay Transaction	Enabled Disabled	This feature is used to meet the latency of PCI cycles to and from the ISA bus. The ISA bus is much, much slower than the PCI bus. Thus, PCI cycles to and from the ISA bus take a longer time to complete and this slows the PCI bus down. However, enabling PCI Delayed Transaction enables the chipset's embedded 32-bit posted write buffer to support delayed transaction cycles. This means that transactions to and from the ISA bus are buffered and the PCI bus can be freed to perform other transactions while the ISA transaction is underway. This option should be enabled for better performance and to meet PCI 2.1 specifications. "Disabled" is set only if the PCI cards cannot work properly or if an ISA card that is not PCI 2.1 compliant is used.
VLink Mode Selection	By Auto Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	The North Bridge interface to the South Bridge through a high speed(up to 1GB/Sec)8x, 66MHz Data Transfer interconnect bus caller "V-Link". This item allows you to select the V-Link mode from 0 to 4.
VLink 8X Support	Enabled Disabled	The feature is to toggle the V-Link bus mode between the original V-Link and the newer and faster 8X V-Link.
DDRY_Timing	Slowest Default Optimize	This item allows you to set the DDRY timing.

3.5.3.4 Memory Hole

This feature allows you to create a memory hole.

Item	Description
512K-640K	When this item is enabled, ISA ROM will be mapped to 15-16M area and also support legacy ISA devices. While this item is disabled and legacy ISA devices are not utilized, the graphic performance will be enhanced

3.5.3.5 System BIOS Cacheable

This feature is only valid when the system BIOS is shadowed. It enables or disables the caching of the system BIOS ROM at **F0000h-FFFFFh** via the L2 cache. This greatly speeds up accesses to the system BIOS. However, this does **not** translate into better system performance because the OS does not need to access the system BIOS much.

Item	Description
Enabled	Cacheable
Disabled	Non-Cacheable

3.5.3.6 Video RAM Cacheable

It enables or disables the caching of the video RAM at **A0000h-AFFFFh**. This greatly speeds up the video performance.

Item	Description
Enabled	Cacheable
Disabled	Non-Cacheable

3.5.3.7 Init Display First

This item allows you to decide to active whether PCI Slot or Onboard/AGP first. The choices: PCI Slot, Onboard, AGP.

3.5.4 Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

Phoenix - AwardBIOS CMOS Setup Utility Integrated Peripherals			
VIA OnChip IDE Device		Item Help	
 VIA OnChip PCI Device SuperIO Device USB Device Setting Onboard Lan Boot ROM 	[Press Enter] [Press Enter]	Menu Level 🕨	
1↓→+:Move Enter:Select E5: Previous Values	+/-/PU/PD:Value F10:Save F6: Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults	

3.5.4.1 VIA OnChip IDE Device

Phoenix - AwardBIOS CMOS Setup Utility VIA OnChip IDE Device		
SATA Controller SATA Controller Mode IDE DMA transfer access OnChip IDE Channel0 OnChip IDE Channel1 IDE Prefetch Mode Primary Master PIO Primary Slave PI0	[<mark>Enabled]</mark> [RAID] [Enabled] [Enabled] [Enabled] [Enabled] [Auto] [Auto]	Item Help Menu Level ►►
Secondary Master PIO Secondary Slave PIO Primary Master UDMA Primary Slave UDMA Secondary Master UDMA Secondary Slave UDMA IDE HDD Block Mode		
	-/PU/PD:Value F10:Save 6: Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults

ltem	Options	Description
SATA Controller	Enabled Disabled	The chipset contains a SATA IDE interface with support for two IDE channels. Select Enabled to activate the primary IDE interface (Channel0). Select Disabled to deactivate this interface.
SATA Mode	IDE RAID	Setup the onboard SATA Mode.
IDE DMA transfer access	Enabled Disabled	This feature allows you to enable or disable DMA support for all IDE devices.
OnChip IDE Channel10/11	Enabled Disabled	The chipset contains a PCI IDE interface with support for two IDE channels. Select Enabled to activate the primary / secondary IDE interface (Channel 10/11). Select Disabled to deactivate this interface.
IDE Prefetch Mode	Enabled Disabled	For faster drive accesses. If you install a primary and/or secondary add-in IDE interface, set this field to Disabled if the interface does not support prefetching.
IDE Primary Master PIO IDE Primary Slave PIO IDE Secondary Master PIO IDE Secondary Slave PIO	Auto Mode 0 Mode 1 Mode 2 Mode 3 Mode 4	The IDE PIO (Programmed Input/Output) fields let you set a PIO mode (0-4) for each of the four IDE devices that the onboard IDE interface supports. Modes 0 through 4 provide successively increased performance. In Auto mode, the system automatically determines the best mode for each device.
IDE Primary Master UDMA IDE Primary Slave UDMA IDE Secondary Master UDMA IDE Secondary Slave UDMA	Auto Disabled	Ultra DMA implementation is possible only if your IDE hard drive supports it and the operating environment includes a DMA driver (Windows 95 OSR2 or a third-party IDE bus master driver). If the hard drive and the system software both support Ultra DMA, select Auto to enable BIOS support.
IDE HDD Block Mode	Enabled Disabled	Block mode is also called block transfer, multiple commands, or multiple sector read/write. If the IDE hard drive supports block mode (most new drives do), select Enabled for automatic detection of the optimal number of block read/writes per sector the drive can support.

3.5.4.2 VIA OnChip PCI Device

Phoenix - AwardBIOS CMOS Setup Utility VIA OnChip PCI Device			
AC97 Audio Controller [Auto]	Item Help		
	Menu Level 🛛 🕨		
	ESC:Exit F1:General Help F7: Optimized Defaults		

Item	Options	Description
AC97 Audio Controller	Disabled	This item allows you to decide to enable/disable the VIA chipset family to support AC97 Audio.

3.5.4.3 Super IO Device

Phoenix -	AwardBIOS CMOS Setup U SuperIO Device	tility
Onboard Serial Port 1	[3F8/IR04]	Item Help
Onboard Serial Port 2 COM PORT 232/422/485 Watch Dog Function × Watch Dog Timer Sel(Min) Onboard Fast IR × Fast IR IRQ × Fast IR DMA	[2F8/IRQ3] [RS232] [Disabled] 1 [Disabled] 11 6	Menu Level 🕨
	/PU/PD:Value F10:Save : Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults

ltem	Options	Description
Onboard Serial Port 1 Onboard Serial Port 2	Disable 3F8/IRQ4 2F8/IRQ3 3E8/IRQ4 2E8/IRQ3 AUTO	Select an address and corresponding interrupt for the first and second serial ports.
COM Port 232/422/485	RS232 RS422 RS485	Select COM port type.
Watch Dog Function:	Enabled Disabled	This item is to set the Watch Dog function Enabled/Disabled.
Watch Dog Timer <min>:</min>	1	This item is to set the timer of Watch Dog function.
Onboard Fast IR:	Enabled Disabled	This item is to set the Onboard Fast IR function Enabled/ Disabled.
Fast IR IRQ:	11, 5 3, 4	Select a corresponding interrupt for Fast IR.
Fast IR DMA:	6, 5	Select a DMA channel for Fast IR.

3.5.4.4 USB Device Setting

	USB Device Setting	-
USB 1.0 Controller	[Enabled]	Item Help
USB 2.0 Controller	[Enabled]	Menu Leuel ►►
USB Operation Mode USB Kevboard Function	[High Speed] [Enabled]	Menu Level 🕨
USB Mouse Function	[Enabled]	[Enable] or [Disable]
	[Enabled]	Universal Host
		Controller
*** USB Mass Storage De	vice Boot Setting ***	Interfacefor Universal
UFDDA	USB Floppy	Serial Bus.
UFDDB	USB Floppy	
No Device	[Auto mode]	
No Device	[Auto mode]	
No Device No Device	[Auto mode] [Auto mode]	
No Device	[Auto mode]	
No Device	[Auto mode]	
No Device	[Auto mode]	
No Device	[Auto mode]	
	/-/PU/PD:Value F10:Save F6: Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults

Item	Options	Description
USB 1.0 Controller	Enabled Disabled	This item is to enable or disable the USB 1.0 Controller.
USB 2.0 Controller	Enabled Disabled	This item is to enable or disable the USB 2.0 Controller.
USB Operation Mode	Full/Low Speed High Speed	This item is to set the speed of USB operation.
USB Keyboard Function	Enabled Disabled	This item is to enable or disable the USB keyboard function.
USB Mouse Function	Enabled Disabled	This item is to enable or disable the USB mouse function.
USB Storage Function	Enabled Disabled	This item is to enable or disable the USB storage function.

3.5.5 Power Management Setup

The Power Management Setup allows you to configure you system to most effectively save energy while operating in a manner consistent with your own style of computer use.

Phoenix - AwardBIOS CMOS Setup Utility Power Management Setup		
ACPI function	[Enabled]	Item Help
Suspend Mode Video Off Option Video Off Method MODEM Use IRO Soft-Off by PWRBTN Run VGABIOS if S3 Resume	[Disable] [Disable] [Suspend -> Off] [V/H SYNC+Blank] [3] [Instant-Off] [Auto] [Off]	Menu Level 🕨
1↓→+:Move Enter:Select +/- F5: Previous Values F6	/PU/PD:Value F10:Save : Fail-Safe Defaults	ESC:Exit F1:General Help F7: Optimized Defaults

3.5.5.1 ACPI Function

This item allows you to enable/disable the ACPI function.

The choices: Enable, Disable.

3.5.5.2 ACPI Suspend Type

This item allows you to select ACPI suspend type.

The choices: S1 (POS), S3 (STR), S1&S3

3.5.5.3 Power Management Option

This category allows you to select the type (or degree) of power saving and is directly related to the following modes:

-	
Item	Description
Min. Power Saving	Minimum power management, HDD Power Down = 15 Min,
Max. Power Saving	Maximum power management, HDD Power Down =1 Min,
User Defined	Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr. except for HDD Power Down which ranges from 1 min. to 15 min. and disable.

3.5.5.4 HDD Power Down

There are three selections for Power Management Option; both of them have fixed mode settings.

The choices: Disabled, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15 Min.

3.5.5.5 Suspend Mode

This setting defines the number of minutes before the system enters "suspend mode", the deepest level of system inactivity shutdown. The exact definition depends on the system, but in general this mode means that all system devices are shutdown (except for any that the BIOS is specifically told to keep running) and the processor is shut down to a trickle mode..

The choices: Disabled, 1, 2, 4, 6, 8, 10, 20, 30, 40 Min, 1 Hour.

3.5.5.6 Video Off Option

This determines the manner in which the monitor is always on or turned off during suspend mode.

The choices: Always On, Suspend -> Off.

3.5.5.7 Video Off Method

This item allows you to select the video off method.

The choices: Blank Screen, V/H SYNC+Blank, DPMS Support

3.5.5.8 MODEM Use IRQ

This determines the IRQ in which the MODEM can use.

The choices: NA, 3, 4, 5, 7, 9, 10, 11.

3.5.5.9 Soft-Off by PWRBTN

Pressing the power button for more than 4 seconds forces the system to enter the Soft-Off state when the system has "hung".(Only could working on ATX Power supply) The choices: Delay 4 Sec, Instant-Off.

3.5.5.10 Run VGABIOS if S3 Resume

This item is to set whether to run VGABIOS if S3 resume.

The choices: Auto, Yes, No

3.5.5.11 Ac Loss Auto Restart:

This item is to set whether to run Ac Loss Auto Restart.

The choices: Off, On, Former-Sts.

3.5.5.12 Wakeup Event Detect

Phoenix -	- AwardBIOS CMOS Setup Ut Wakeup Event Detect	ility
PS2KB Wakeup Select	[Hot key]	Item Help
PS2KB Wakeup Key select PS2MS Wakeup Key Select PS2 Keyboard Power ON PS2 Mouse Power ON PowerOn by PCI Card Modem Ring Resume RTC Alarm Resume × Date (of Month) × Resume Time (hh:mm:ss)	[Any Key] [Any Button] [Disabled] [Disabled] [By OS] [Disabled] 0 : 25 : 0	Menu Level When Select Password, Please press ENTER key to change Password Max 8 numbers.
		ESC:Exit F1:General Help F7: Optimized Defaults

Item	Option	Description	
DS2KD Wakoup Salaat	Hot Key	Allows you to select the method of PS2KB wakeup	
PS2KB Wakeup Select	Password	Allows you to select the method of PS2RB wakeup	
	Ctrl + F1~F12		
PS2KB Wakeup Key Select	Power	Allows you to set the key of PS2 keyboard wakeup	
FOZNE Wakeup Ney Select	Wake	Allows you to set the key of FS2 keyboard wakeup	
	Any Key		
	Any Button		
PS2KB Wakeup Key Select	Left Button	Allows you to set the key of PS2 mouse wakeup	
	Right Button		
PS2 Keyboard Power On	Disabled	Allows you to enable or disable PS2 keyboard power on	
	Enabled	Allows you to enable or disable PS2 keyboard power	
PS2 Mouse Power On	Disabled	Allows you to enable or disable PS2 Mouse power on	
PS2 Mouse Power On	Enabled	Allows you to enable of disable P32 wouse power of	
PowerOn by PCI Card	By OS	Allows you to set power on by PCI card	
	Enabled	Allows you to set power on by P Cr card	
Modem Ring Reume	By OS	Allows you to resume modem ring	
	Enabled	Allows you to resume modem ring	
RTC Alarm Resume	Disabled	Allows you to enable or disable RTC alarm	
	Enabled		
Date (of Month)	0	Not applicable with RTC Alarm Resume disabled	
Resume Time (hh:mm:ss)	0	Not applicable with RTC Alarm Resume disabled	

3.5.6 PnP / PCI Configuration

This section describes configuring the PCI bus system. PCI, or **P**ersonal **C**omputer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components. This section covers some very technical items and it is strongly recommended that only experienced users should make any changes to the default settings.

Phoenix - AwardBIOS CMOS Setup Utility PnP/PCI Configurations		
PNP OS Installed Reset Configuration Data Resources Controlled By X IRQ Resources PCI/VGA Palette Snoop Assign IRQ For VGA Assign IRQ For USB ** PCI Express relative i Maximum ASPM supported Maximum Payload Size	[Auto(ESCD)] Press Enter [Disabled] [Enabled] [Enabled] tems ** [LØs&L1]	Item Help Menu Level ► Select Yes if you are using a Plug and Play capable operating system Select No if you need the BIOS to configure non-boot devices
↑↓→+:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults		

3.5.6.1 PNP OS Installed

The choices: Yes, No.

3.5.6.2 Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

The choices: Enabled, Disabled.

3.5.6.3 Resources Controlled By

The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows®95. If you set this field to "manual" choose specific resources by going into each of the sub menu that follows this field (a sub menu is preceded by a ">").

The choices: Auto(ESCD), Manual.

3.5.6.4 IRQ Resource

When resources are controlled manually, assign each system interrupt a type, depending on the type of device using the interrupt.

This item allows you to determine the IRQ assigned to the PCI bus or reserved.

The Choices: PCI, Reserved.

IRQ-3 assigned to	[PCI Device]	Item Help
IRQ-4 assigned to IRQ-5 assigned to IRQ-7 assigned to IRQ-9 assigned to IRQ-10 assigned to IRQ-11 assigned to IRQ-12 assigned to IRQ-14 assigned to IRQ-15 assigned to	[PCI Device] [PCI Device] [PCI Device] [PCI Device] [PCI Device] [PCI Device] [PCI Device] [PCI Device] [PCI Device]	Menu Level Legacy ISA for devices compliant with the original PC AT bus specification, PCI/ISA PnP for devices compliant with the Plug and Play standard whether designed for PCI or ISA bus architecture

3.5.6.5 PCI / VGA Palette Snoop

Leave this field at Disabled.

The choices: Enabled, Disabled.

3.5.6.6 Assign IRQ For VGA

While the system has one VGA controller and more than one VGA devices are connected, then "Enabled" is set. If the system VGA controller is not used, then "Disabled" is set. The choices: Enabled, Disabled.

3.5.6.7 Assign IRQ For USB

While the system has one USB controller and more than one USB devices are connected, then "Enabled" is set. If the system USB controller is not used, then "Disabled" is set. The choices: Enabled, Disabled.

3.5.6.8 Maximum ASPM supported

This item is used to control the maximum level of supported ASPM on the given PCI Express link on the system.

The choices: L0, L0s, L1, L0s&L1.

3.5.6.9 Maximum Payload Size

This item is used to select the maximum TLP payload size of the PCI Express devices. The unit is byte.

The choices: 128, 256, 512, 1024, 2048, 4096.

3.5.7 PC Health Status

This section shows the status of your CPU.

Phoenix - AwardBIOS CMOS Setup Utility PC Health Status		
Current CPU Temp	Item Help	
3.3V 1.8VDIMM 1.5VDD VCore Internal Vcc	Menu Level 🕨	
	ESC:Exit F1:General Help F7: Optimized Defaults	

3.5.8 Frequency / Voltage Control

This menu specifies your setting for frequency/voltage control.



3.5.8.1 CPU Clock Ratio:

This item allows you to select the CPU clock ratio.

The choices: 6X

3.5.8.2 Auto Detect PCI Clk

This item allows you to enable or disable detecting PCI clock automatically.

The choices: Enabled, Disabled.

3.5.8.3 Spread Spectrum

This item is to adjust extreme values of the pulse for EMI test.

The choices: Enabled, Disabled.

3.5.8.4 CPU Clock

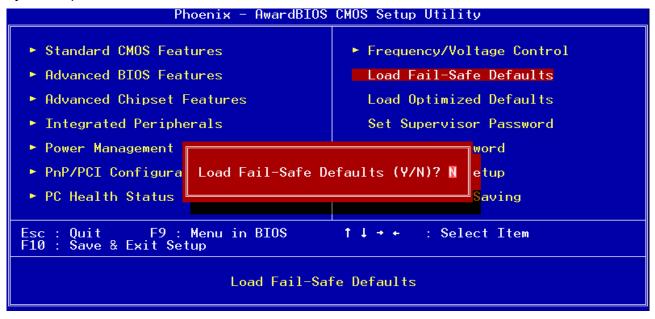
This item allows you to select the CPU clock.

The choices: 100.

3.5.9 Load Fail-Safe Defaults

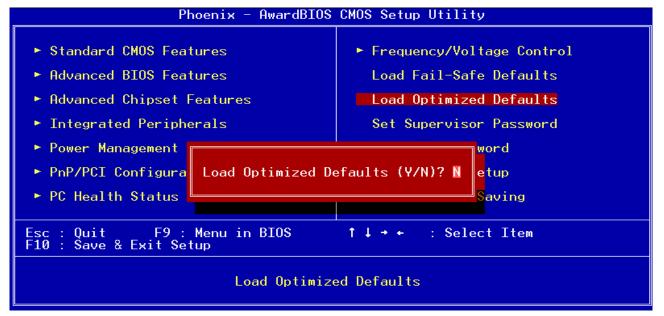
Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

Press <Y> to load the BIOS default values for the most stable, minimal-performance system operations.



3.5.10 Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs. Press <Y> to load the default values setting for optimal performance system operations.



ECM-3711 Series

3.5.11 Set Supervisor / User Password

You can set either supervisor or user password, or both of them. Supervisor Password: able to enter/change the options of setup menus.



User Password: able to enter but no right to change the options of setup menus.

Phoenix - AwardBIOS CMOS Setup Utility		
 Standard CMOS Features Advanced BIOS Features Advanced Chipset Features Integrated Peripherals Power Management Setup PnP/PCI Configurati PC Health Status 	 Frequency/Voltage Control Load Fail-Safe Defaults Load Optimized Defaults Set Supervisor Password Set User Password t Setup ut Saving 	
Esc : Quit F9 : Menu in BIOS ↑↓ → ← : Select Item F10 : Save & Exit Setup Change/Set/Disable Password		

Type the password, up to eight characters in length, and press <Enter>. The password typed now will clear any previously entered password from CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

PASSWORD DISABLED.

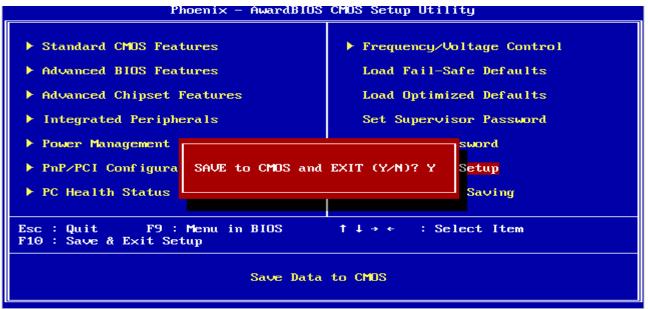
When a password has been enabled, you will be prompted to enter it every time you try to enter Setup. This prevents an unauthorized person from changing any part of your system configuration. Additionally, when a password is enabled, you can also require the BIOS to request a password every time your system is rebooted. This would prevent unauthorized use of your computer. You determine when the password is required within the BIOS Features Setup Menu and its Security option (see Section 3). If the Security option is set to "System", the password will be required both at boot and at entry to Setup. If set to "Setup", prompting only occurs when trying to enter Setup

3.5.12 Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

Enter <Y> to store the selection made in the menus in CMOS, a special section in memory that stays on after turning the system off. The BIOS configures the system according to the Setup selection stored in CMOS when boot the computer next time.

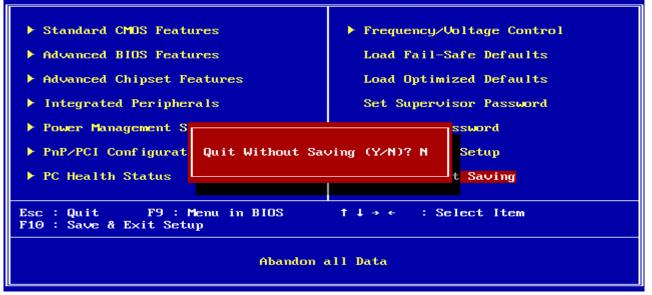
The system is restarted after saving the values.



3.5.13 Exit Without Save

Abandon all CMOS value changes and exit setup, and the system is restarted after exiting.

Phoenix - AwardBIOS CMOS Setup Utility



User's Manual

4. Drivers Installation



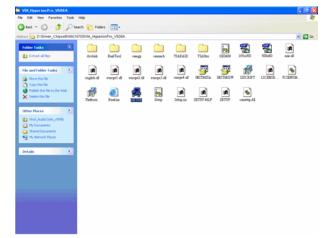
Note: Installation procedures and screen shots in this section are for your reference and may not be exactly the same as shown on your screen.

4.1 Install Chipset Driver (For VIA CN700)

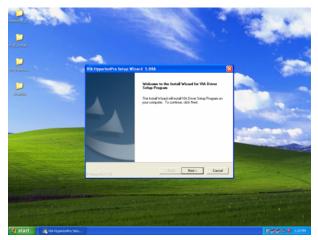
Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Chipset\VIA\CN700.**



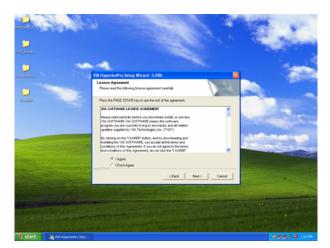
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



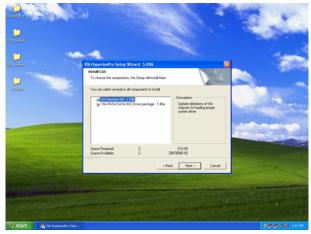
Step 1. Locate \Driver_Audio\VIA\CN700\VIA_HyperionPro_V508A\setup.exe].



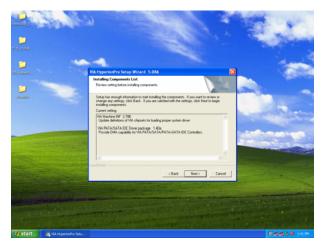
Step 2. Click Next.



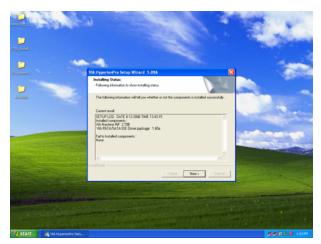
Step 3. Select **I Agree** and click **Next** to the following step.



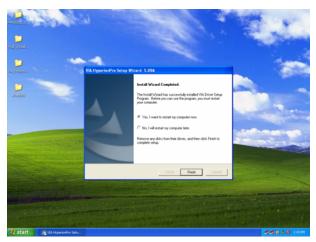
Step 4. Select both items and click **Next** to run the setup.



Step 5. Click Next.



Step 6. Click Next.



Step 7. Click Finish to restart the PC.

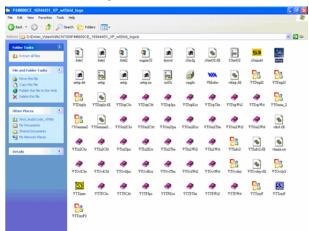
4.2 Install Display Driver (For VIA CN700)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to

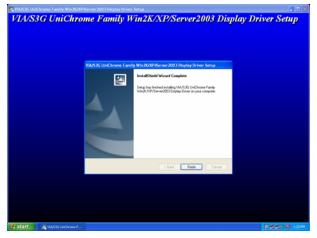
\Driver_Display\VIA\CN700.



Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



Step1. Locate 「\Driver_Chipset\VIA \CN700\P4M800CE_16944451_XP _wIShId_logod\Setup.exe」.



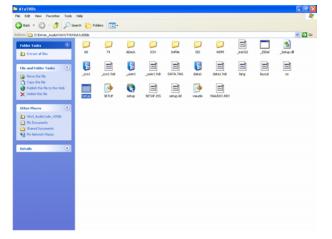
Step 2. Setup will run the installation automatically, then click **Finish** to complete.

4.3 Install Audio Driver (For VIA VT1616)

Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to **\Driver_Audio\VIA\VT1616.**



Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



Step 1. Locate \Driver_Audio\VIA\VT1616 \A1u590b\setup.exe _ .



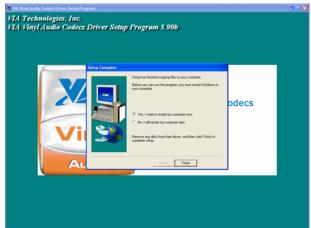
Step 2. Click Next.



Step 3. Select **Install Driver** and click **Next** to the following step.



Step 4. Click Continue Anyway to run the setup.



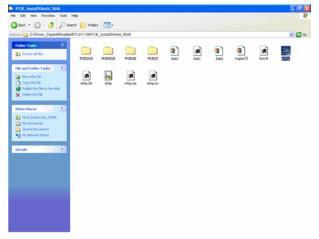
Step 5. Click **Finish** to complete the setup and restart the PC.

4.4 Install Ethernet Driver (For Realtek RTL8111B)

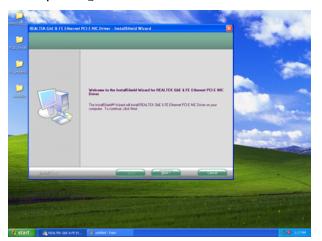
Insert the Supporting CD-ROM to CD-ROM drive, and it should show the index page of Evalue's products automatically. If not, locate Index.htm and choose the product from the menu left, or link to D:\Driver_Gigabit\Realtek\ RTL8111B.



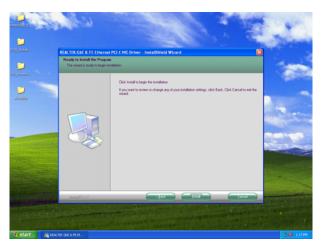
Note: The installation procedures and screen shots in this section are based on Windows XP operation system.



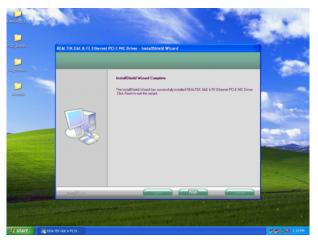
Step 1. Locate 「\Driver_Gigabit\Realtek\ RTL8111B\PCIE_InstallShield_5646 \Setup.exe_.



Step 2. Click Next.

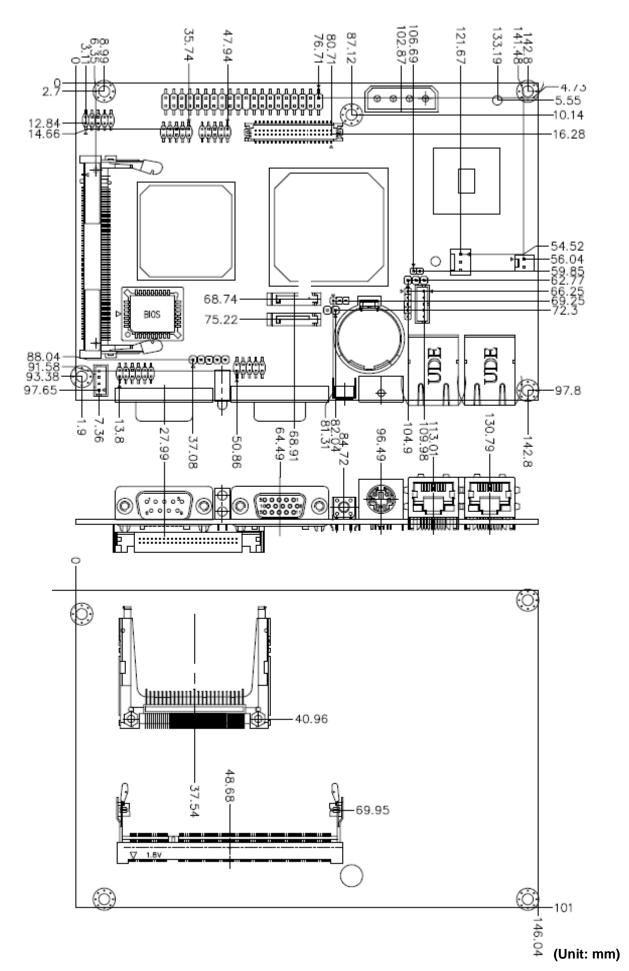


Step 3. Click Next to run the installation.



Step 4. Click **Finish** to complete the setup.

5. Measurement Drawing



Appendix A: BIOS Revisions

BIOS Rev.

New Features

Bugs/Problems Solved

Known Problems

Appendix B: AWARD BIOS POST Messages

Overview

During the Power On Self-Test (POST), if the BIOS detects an error requiring you to do something to fix, it will either sound a beep code or display a message.

If a message is displayed, it will be accompanied by:

PRESS F1 TO CONTINUE, CTRL-ALT-ESC OR DEL TO ENTER SETUP

Post Beep

Currently there are two kinds of beep codes in BIOS. This code indicates that a video error has occurred and the BIOS cannot initialize the video screen to display any additional information. This beep code consists of a single long beep followed by two short beeps. The other code indicates that your DRAM error has occurred. This beep code consists of a single long beep repeatedly.

Error Messages

One or more of the following messages may be displayed if the BIOS detects an error during the POST. This list includes messages for both the ISA and the EISA BIOS.

1. CMOS BATTERY HAS FAILED

CMOS battery is no longer functional. It should be replaced.

2. CMOS CHECKSUM ERROR

Checksum of CMOS is incorrect. This can indicate that CMOS has become corrupt. This error may have been caused by a weak battery. Check the battery and replace if necessary.

3. DISK BOOT FAILURE, INSERT SYSTEM DISK AND PRESS ENTER

No boot device was found. This could mean that either a boot drive was not detected or the drive does not contain proper system boot files. Insert a system disk into Drive A: and press <Enter>. If you assumed the system would boot from the hard drive, make sure the controller is inserted correctly and all cables are properly attached. Also be sure the disk is formatted as a boot device. Then reboot the system.

4. DISKETTE DRIVES OR TYPES MISMATCH ERROR - RUN SETUP

Type of diskette drive installed in the system is different from the CMOS definition. Run Setup to reconfigure the drive type correctly.

5. DISPLAY SWITCH IS SET INCORRECTLY

Display switch on the motherboard can be set to either monochrome or color. This indicates the switch is set to a different setting than indicated in Setup. Determine which setting is correct, and then either turn off the system and change the jumper, or enter Setup and change the VIDEO selection.

6. DISPLAY TYPE HAS CHANGED SINCE LAST BOOT

Since last powering off the system, the display adapter has been changed. You must configure the system for the new display type.

7. EISA Configuration Checksum Error

PLEASE RUN EISA CONFIGURATION UTILITY

The EISA non-volatile RAM checksum is incorrect or cannot correctly read the EISA slot. This can indicate either the EISA non-volatile memory has become corrupt or the slot has been configured incorrectly. Also be sure the card is installed firmly in the slot.

8. EISA Configuration Is Not Complete

PLEASE RUN EISA CONFIGURATION UTILITY

The slot configuration information stored in the EISA non-volatile memory is incomplete.



Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

9. ERROR ENCOUNTERED INITIALIZING HARD DRIVE

Hard drive cannot be initialized. Be sure the adapter is installed correctly and all cables are correctly and firmly attached. Also be sure the correct hard drive type is selected in Setup.

10. ERROR INITIALIZING HARD DISK CONTROLLER

Cannot initialize controller. Make sure the cord is correctly and firmly installed in the bus. Be sure the correct hard drive type is selected in Setup. Also check to see if any jumper needs to be set correctly on the hard drive.

11. FLOPPY DISK CNTRLR ERROR OR NO CNTRLR PRESENT

Cannot find or initialize the floppy drive controller. Make sure the controller is installed correctly and firmly. If there are no floppy drives installed, be sure the Diskette Drive selection in Setup is set to NONE.

12. Invalid EISA Configuration

PLEASE RUN EISA CONFIGURATION UTILITY

The non-volatile memory containing EISA configuration information was programmed incorrectly or has become corrupt. Re-run EISA configuration utility to correctly program the memory.



Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

13. KEYBOARD ERROR OR NO KEYBOARD PRESENT

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

If you are purposely configuring the system without a keyboard, set the error halt condition in Setup to HALT ON ALL, BUT KEYBOARD. This will cause the BIOS to ignore the missing keyboard and continue the boot.

14. Memory Address Error at ...

Indicates a memory address error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

15. Memory parity Error at ...

Indicates a memory parity error at a specific location. You can use this location along with the memory map for your system to find and replace the bad memory chips.

16. MEMORY SIZE HAS CHANGED SINCE LAST BOOT

Memory has been added or removed since the last boot. In EISA mode use Configuration Utility to reconfigure the memory configuration. In ISA mode enter Setup and enter the new memory size in the memory fields.

17. Memory Verify Error at ...

Indicates an error verifying a value already written to memory. Use the location along with your system's memory map to locate the bad chip.

18. OFFENDING ADDRESS NOT FOUND

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem cannot be isolated.

19. OFFENDING SEGMENT:

This message is used in conjunction with the I/O CHANNEL CHECK and RAM PARITY ERROR messages when the segment that has caused the problem has been isolated.

20. PRESS A KEY TO REBOOT

This will be displayed at the bottom screen when an error occurs that requires you to reboot. Press any key and the system will reboot.

21. PRESS F1 TO DISABLE NMI, F2 TO REBOOT

When BIOS detects a Non-maskable Interrupt condition during boot, this will allow you to disable the NMI and continue to boot, or you can reboot the system with the NMI enabled.

22. RAM PARITY ERROR - CHECKING FOR SEGMENT ...

Indicates a parity error in Random Access Memory.

23. Should Be Empty But EISA Board Found

PLEASE RUN EISA CONFIGURATION UTILITY

A valid board ID was found in a slot that was configured as having no board ID.



Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

24. Should Have EISA Board But Not Found

PLEASE RUN EISA CONFIGURATION UTILITY

The board installed is not responding to the ID request, or no board ID has been found in the indicated slot.



Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

25. Slot Not Empty

Indicates that a slot designated as empty by the EISA Configuration Utility actually contains a board.



Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

26. SYSTEM HALTED, (CTRL-ALT-DEL) TO REBOOT ...

Indicates the present boot attempt has been aborted and the system must be rebooted. Press and hold down the CTRL and ALT keys and press DEL.

27. Wrong Board In Slot

PLEASE RUN EISA CONFIGURATION UTILITY

The board ID does not match the ID stored in the EISA non-volatile memory.



Note: When either of these errors appears, the system will boot in ISA mode, which allows you to run the EISA Configuration Utility.

- 28. FLOPPY DISK(S) fail (80) \rightarrow Unable to reset floppy subsystem.
- 29. FLOPPY DISK(S) fail (40) \rightarrow Floppy Type dismatch.
- 30. Hard Disk(s) fail (80) \rightarrow HDD reset failed.
- 31. Hard Disk(s) fail (40) \rightarrow HDD controller diagnostics failed.
- 32. Hard Disk(s) fail (20) \rightarrow HDD initialization error.
- 33. Hard Disk(s) fail (10) \rightarrow Unable to recalibrate fixed disk.
- 34. Hard Disk(s) fail (08) \rightarrow Sector Verify failed.
- 35. Keyboard is locked out Unlock the key.

BIOS detect the keyboard is locked. P17 of keyboard controller is pulled low.

36. Keyboard error or no keyboard present.

Cannot initialize the keyboard. Make sure the keyboard is attached correctly and no keys are being pressed during the boot.

37. Manufacturing POST loop.

System will repeat POST procedure infinitely while the P15 of keyboard controller is pull low. This is also used for M/B burn in test.

38. BIOS ROM checksum error - System halted.

The checksum of ROM address F0000H-FFFFFH is bad.

39. Memory test fail.

BIOS reports the memory test fail if the onboard memory is tested error.

40. POST Codes

POST (hex)	Description
CFh	Test CMOS R/W functionality.
	Early chipset initialization:
C0h	-Disable shadow RAM
	-Disable L2 cache (socket 7 or below)
	-Program basic chipset registers
	Detect memory
C1h	-Auto-detection of DRAM size, type and ECC.
	-Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen
0311	2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface
0/11	2. Initialize 8042 self-test
	1. Test special keyboard controller for Winbond 977 series Super I/O
08h	chips.
	2. Enable keyboard interface.
09h	Reserved
	1. Disable PS/2 mouse interface (optional).
0Ah	2. Auto detect ports for keyboard & mouse followed by a port & interface
07.11	swap (optional).
	3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved
0Dh	Reserved
0Eh	Test F000h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
	Auto detect flash type to load appropriate flash R/W codes into the run
10h	time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
	Program chipset default values into chipset. Chipset default
14h	values are MODBINable by OEM customers.

POST (hex)	Description
15h	Reserved
16h	Initial Early Init Onboard Generator switch.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or
	Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W
	interrupts are directed to SPURIOUS_INT_HDLR & S/W
	interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY PM INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value:
	e.g. a value of 5Ah is an invalid value for RTC minute.
	2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use
	default value instead.
	3. Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take
	into consideration of the ESCD's legacy information.
	4. Onboard clock generator initialization. Disable respective clock
	resource to empty PCI & DIMM slots.
	5. Early PCI initialization:
	-Enumerate PCI bus number
	-Assign memory & I/O resource
	-Search for a valid VGA device & VGA BIOS, and put it
	into C000:0.
24h	Reserved
25h	Reserved
26h	Reserved
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address.
	2. Initialize the APIC for Pentium class CPU.
	3. Program early chipset according to CMOS setup. Example: onboard IDE controller.
	4. Measure CPU speed. 5. Invoke video BIOS.
2Ah	
	Reserved
2Bh	Reserved
2Ch	Reserved

POST (hex)	Description
	1. Initialize multi-language
2Dh	1. Put information on screen display, including Award title, CPU type,
	CPU speed
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard except Winbond 977 series Super I/O chips.
34h	Reserved
35h	Reserved
36h	Reserved
37h	Reserved
38h	Reserved
39h	Reserved
3Ah	
3Bh	Reserved Reserved
3Ch	
	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
	1. Calculate total memory by testing the last double word of each 64K
49h	page.
	2. Program writes allocation for AMD K5 CPU.
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
	1. Program MTRR of M1 CPU
	2. Initialize L2 cache for P6 class CPU & program CPU with proper
	cacheable range.
4Eh	3. Initialize the APIC for P6 class CPU.
	4. On MP platform, adjust the cacheable range to smaller one in case
	the cacheable ranges between each CPU are not identical.
4Fh	Reserved
50h	Initialize USB
,	

POST (hex)	Description
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Reserved
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved
	1. Display PnP logo
57h	2. Early ISA PnP initialization
••••	-Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
	(Optional Feature)
5Bh	Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
	1. Initialize Init_Onboard_Super_IO switch.
5Dh	2. Initialize Init Onbaord AUDIO switch.
5Eh	Reserved
5Fh	Reserved
	Okay to enter Setup utility; i.e. not until this POST stage can users enter
60h	the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reserved
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
	Prepare memory size information for function call:
67h	INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
	Program chipset registers according to items described in Setup &
6Bh	Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices.
	2. Auto assign ports to onboard COM ports if the corresponding item in
	Setup is set to "AUTO".
6Eh	Reserved
	1. Initialize floppy controller
6Fh	2. Set up floppy related fields in 40:hardware.
70h	Reserved
71h	Reserved
72h	Reserved

POST (hex)	Description
	(Optional Feature)
73h	Enter AWDFLASH.EXE if :
	-AWDFLASH is found in floppy drive.
	-ALT+F2 is pressed
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM
76h	Reserved
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Reserved
7Dh	Reserved
7Eh	Reserved
	1. Switch back to text mode if full screen logo is supported.
	-If errors occur, report errors & wait for keys
7Fh	-If no errors occur or F1 key is pressed to continue:
	Clear EPA or customization logo.
80h	Reserved
81h	Reserved
0111	
82h	1. Call chipset power management hook.
0211	2. Recover the text fond used by EPA logo (not for full screen logo)3. If password is set, ask for password.
0.2.6	
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
	1. USB final Initialization 2. NET PC: Build SYSID structure
	3. Switch screen back to text mode
85h	4. Set up ACPI table at top of memory.5. Invoke ISA adapter ROMs
	6. Assign IRQs to PCI devices
	7. Initialize APM
	8. Clear noise of IRQs.
86h	Reserved
87h	Reserved
88h	Reserved
89h	Reserved
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code

POST (hex)	Description
94h	 Enable L2 cache Program boot up speed Chipset final initialization. Power management final initialization Clear screen & display summary table Program K6 write allocation Program P6 class write combining
95h	1. Program daylight saving 1. Update keyboard LED & typematic rate
96h	 Build MP table Build & update ESCD Set CMOS century to 20h or 19h Load CMOS time into DOS timer tick Build MSIRQ routing table.
FFh	Boot attempt (INT 19h)